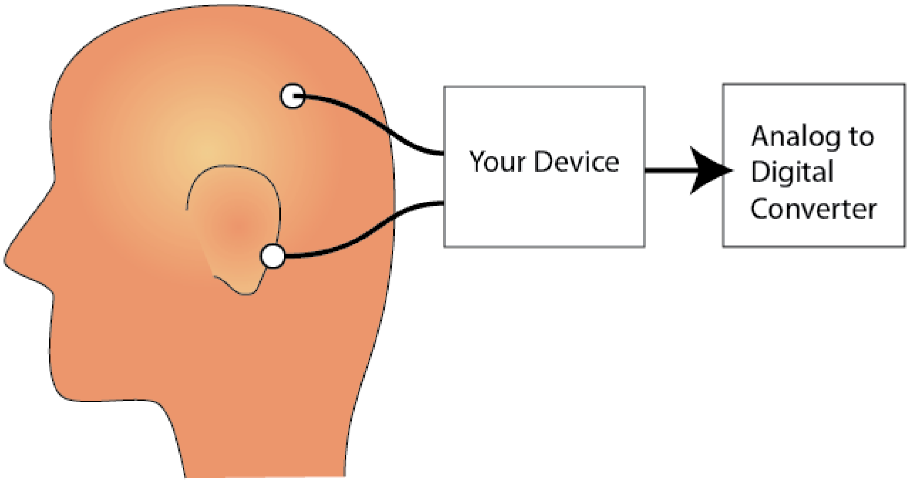
Problem set 2
Due in class April 30

Design an EEG front end according to the following specifications

1. The amplitude of the EEG signal will go up to 200 microVolts and contain features of interest between 1 Hz and 100 Hz.
2. Remember that the electrodes will probably have a contact potential between 10 and 30 mV.
3. Your front end system should act as an input to a 16 bit analog to digital converter with a maximum Voltage swing of ±2.5 Volts (note: this is different than I suggested on the blackboard in class.)
4. If you need a frequency filter, I recommend a second order Sallen-Key design.
5. You will be using an INA114 instrumentation amplifier, and as may TL072 opamps as you need for your filters. I have attached data sheets for these devices.

Have fun. You will learn a lot by doing this.



Resources

Guide to Opamps (really good)
http://focus.ti.com/lit/an/slod006b/slod006b.pdf

Filter design tool:
http://www.analog.com/Analog_Root/static/techSupport/designTools/interactiveTools/filter/filter.html

The OpenEEG project
http://openeeg.sourceforge.net/doc/

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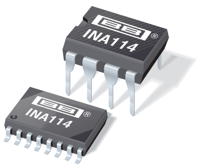


INA114

Precision
INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.25µV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVER-VOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 3mA max
- 8-PIN PLASTIC AND SOL-16

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

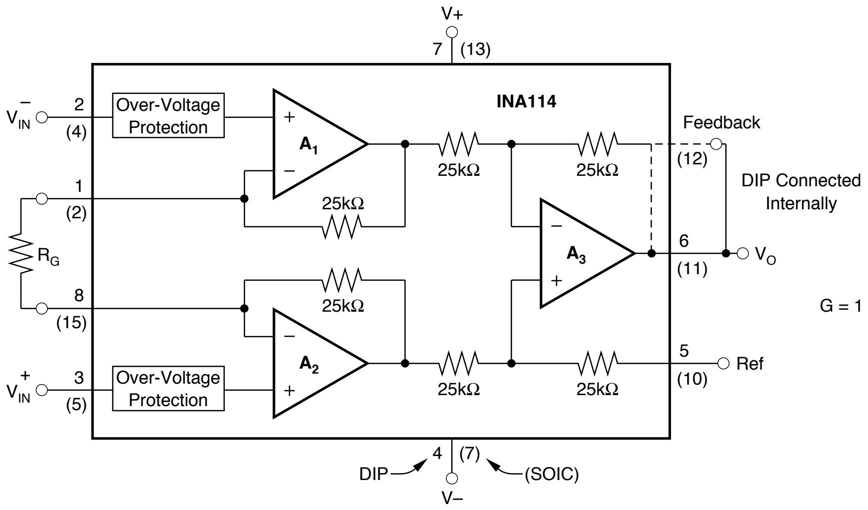
DESCRIPTION

The INA114 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA114 is laser trimmed for very low offset voltage (50µV), drift (0.25µV/°C) and high common-mode rejection (115dB at G = 1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA114 is available in 8-pin plastic and SOL-16 surface-mount packages. Both are specified for the –40°C to +85°C temperature range.



$$G = 1 + \frac{50k\Omega}{R_G}$$

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

Printed in U.S.A. March, 1998

SPECIFICATIONS

ELECTRICAL

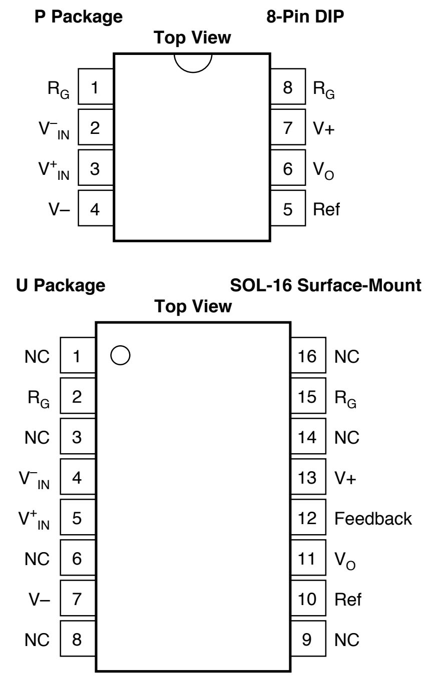
At T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	INA114BP, BU			INA114AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±10 + 20/G	±50 + 100/G		±25 + 30/G	±125 + 500/G	μV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±0.1 + 0.5/G	±0.25 + 5/G		±0.25 + 5/G	±1 + 10/G	μV/°C
vs Power Supply	V_S = ±2.25V to ±18V		0.5 + 2/G	3 + 10/G		✻	✻	μV/V
Long-Term Stability			±0.2 + 0.5/G			✻		μV/mo
Impedance, Differential			10^{10} ∥ 6			✻		Ω ∥ pF
Common-Mode			10^{10} ∥ 6			✻		Ω ∥ pF
Input Common-Mode Range		±11	±13.5		✻	✻		V
Safe Input Voltage				±40			✻	V
Common-Mode Rejection	V_{CM} = ±10V, ΔR_S = 1kΩ							
	G = 1	80	96		75	90		dB
	G = 10	96	115		90	106		dB
	G = 100	110	120		106	110		dB
	G = 1000	115	120		106	110		dB
BIAS CURRENT			±0.5	±2		✻	±5	nA
vs Temperature			±8			✻		pA/°C
OFFSET CURRENT			±0.5	±2		✻	±5	nA
vs Temperature			±8			✻		pA/°C
NOISE VOLTAGE, RTI	G = 1000, R_S = 0Ω							
f = 10Hz			15			✻		nV/√Hz
f = 100Hz			11			✻		nV/√Hz
f = 1kHz			11			✻		nV/√Hz
f_B = 0.1Hz to 10Hz			0.4			✻		μVp-p
Noise Current								
f=10Hz			0.4			✻		pA/√Hz
f=1kHz			0.2			✻		pA/√Hz
f_B = 0.1Hz to 10Hz			18			✻		pAp-p
GAIN								
Gain Equation			1 + (50kΩ/R_G)			✻		V/V
Range of Gain		1		10000	✻		✻	V/V
Gain Error	G = 1		±0.01	±0.05		✻	✻	%
	G = 10		±0.02	±0.4		✻	±0.5	%
	G = 100		±0.05	±0.5		✻	±0.7	%
	G = 1000		±0.5	±1		✻	±2	%
Gain vs Temperature	G = 1		±2	±10		✻	±10	ppm/°C
50kΩ Resistance(1)			±25	±100		✻	✻	ppm/°C
Nonlinearity	G = 1		±0.0001	±0.001		✻	±0.002	% of FSR
	G = 10		±0.0005	±0.002		✻	±0.004	% of FSR
	G = 100		±0.0005	±0.002		✻	±0.004	% of FSR
	G = 1000		±0.002	±0.01		✻	±0.02	% of FSR
OUTPUT								
Voltage	I_O = 5mA, T_{MIN} to T_{MAX}	±13.5	±13.7		✻	✻		V
	V_S = ±11.4V, R_L = 2kΩ	±10	±10.5		✻	✻		V
	V_S = ±2.25V, R_L = 2kΩ	±1	±1.5		✻	✻		V
Load Capacitance Stability			1000			✻		pF
Short Circuit Current			+20/–15			✻		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		1			✻		MHz
	G = 10		100			✻		kHz
	G = 100		10			✻		kHz
	G = 1000		1			✻		kHz
Slew Rate	V_O = ±10V, G = 10	0.3	0.6		✻	✻		V/μs
Settling Time, 0.01%	G = 1		18			✻		μs
	G = 10		20			✻		μs
	G = 100		120			✻		μs
	G = 1000		1100			✻		μs
Overload Recovery	50% Overdrive		20			✻		μs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	✻	✻	✻	V
Current	V_{IN} = 0V		±2.2	±3		✻	✻	mA
TEMPERATURE RANGE								
Specification		–40		85	✻		✻	°C
Operating		–40		125	✻		✻	°C
θ_{JA}			80			✻		°C/W

✻ Specification same as INA114BP/BU.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

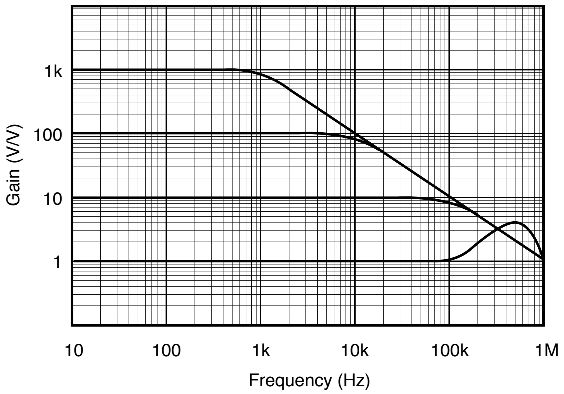
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	TEMPERATURE RANGE
INA114AP	8-Pin Plastic DIP	006	–40°C to +85°C
INA114BP	8-Pin Plastic DIP	006	–40°C to +85°C
INA114AU	SOL-16 Surface-Mount	211	–40°C to +85°C
INA114BU	SOL-16 Surface-Mount	211	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

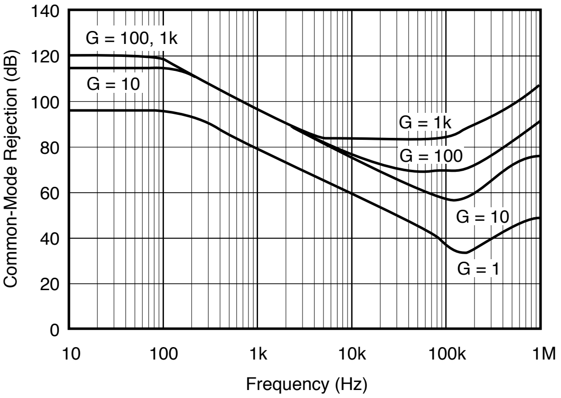
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, $V_S = ±15V$, unless otherwise noted.

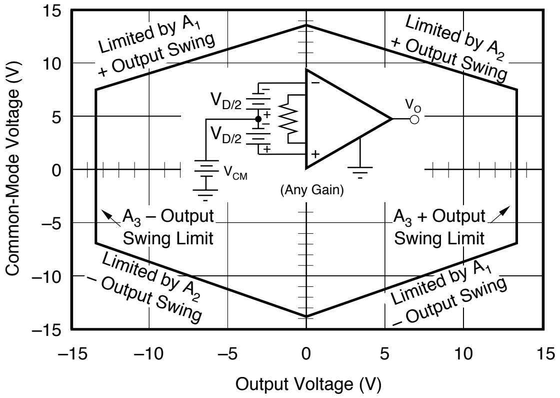
GAIN vs FREQUENCY



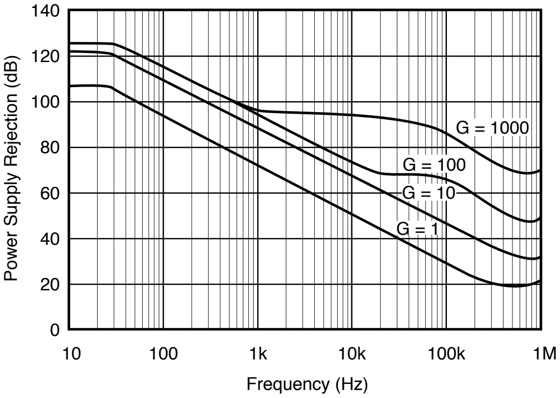
COMMON-MODE REJECTION vs FREQUENCY



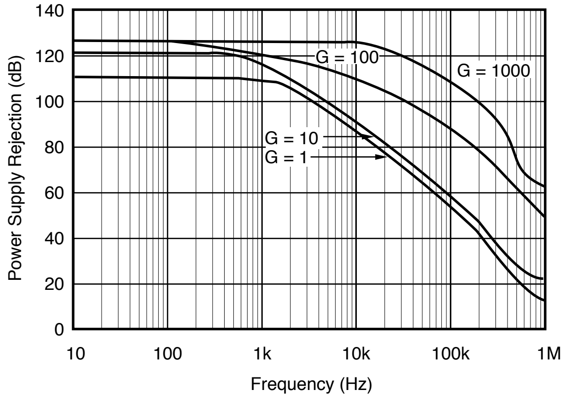
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



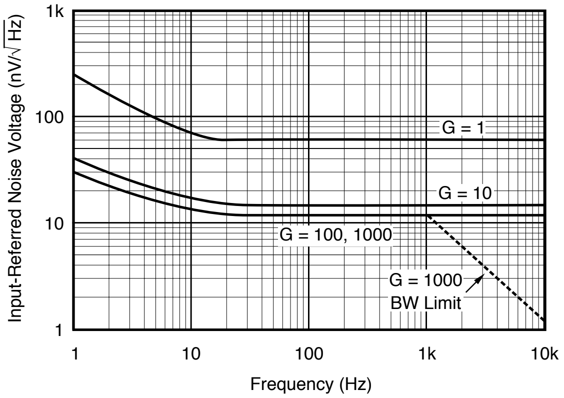
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY

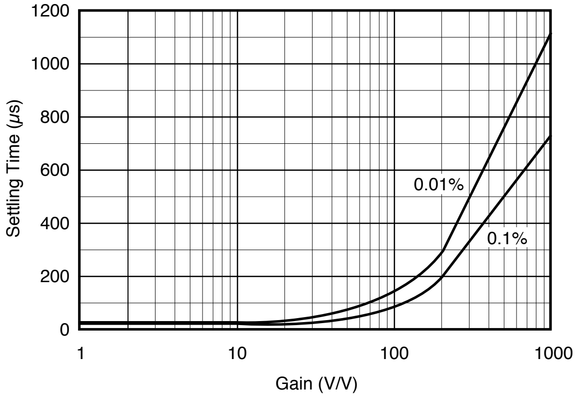


INPUT-REFERRED NOISE VOLTAGE vs FREQUENCY

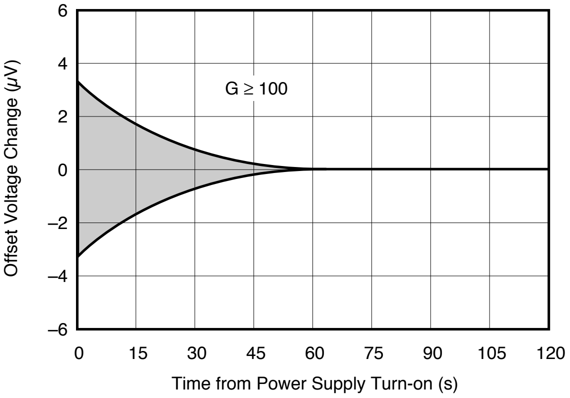


TYPICAL PERFORMANCE CURVES (CONT)

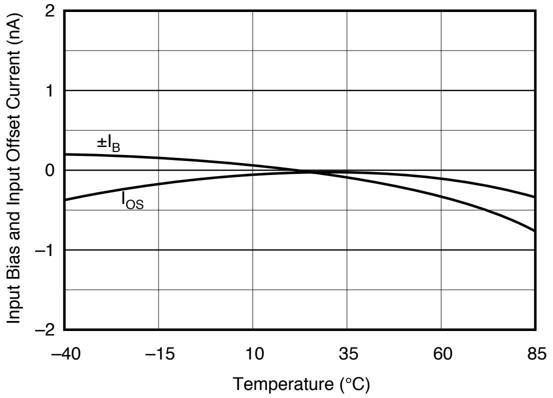
At $T_A = +25°C$, $V_S = ±15V$, unless otherwise noted.



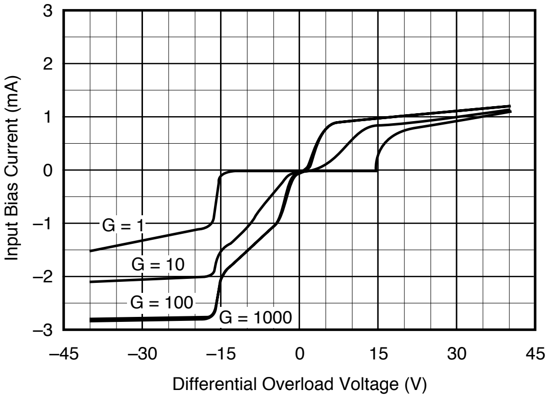
SETTLING TIME vs GAIN



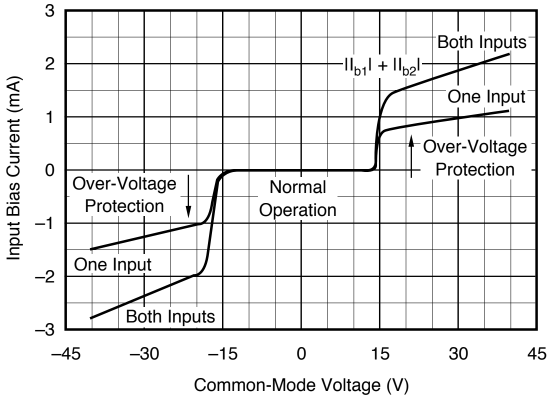
OFFSET VOLTAGE WARM-UP vs TIME



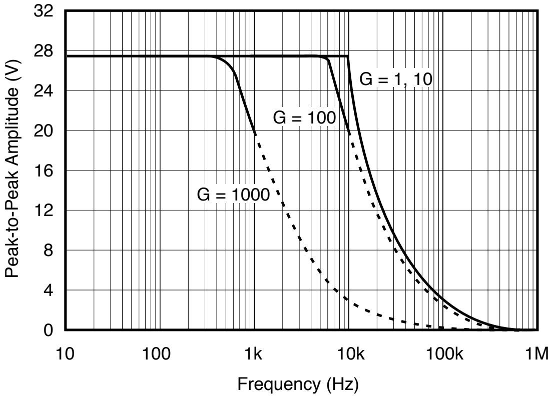
INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

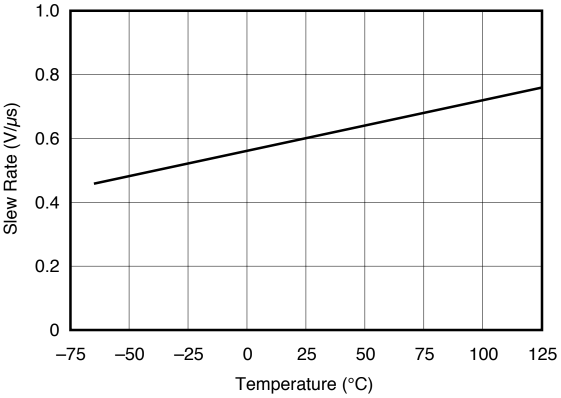


MAXIMUM OUTPUT SWING vs FREQUENCY

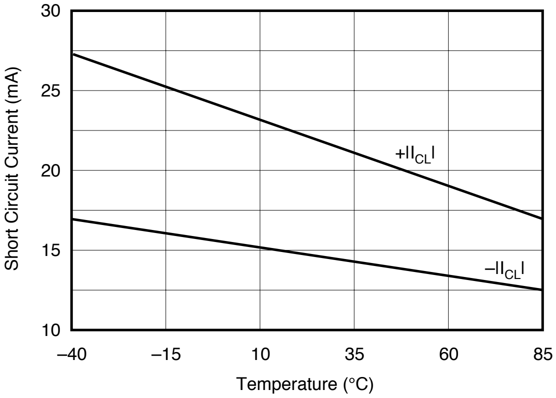
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = ±15V$, unless otherwise noted.

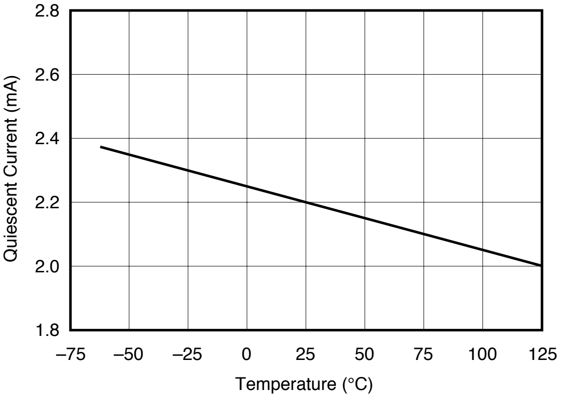
SLEW RATE vs TEMPERATURE



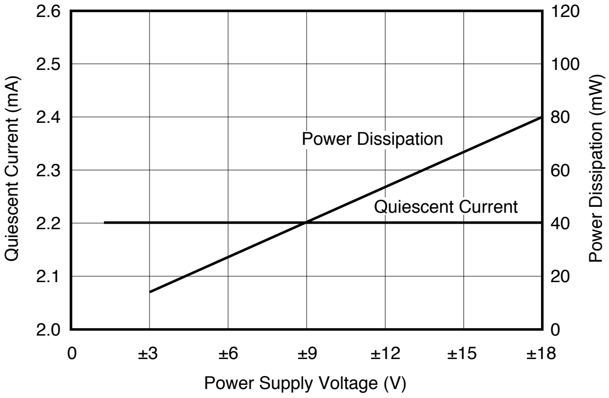
OUTPUT CURRENT LIMIT vs TEMPERATURE



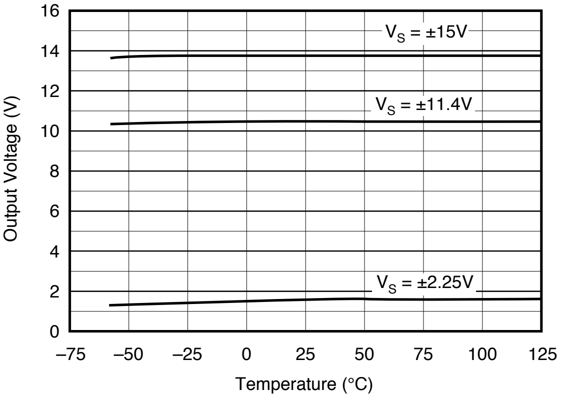
QUIESCENT CURRENT vs TEMPERATURE



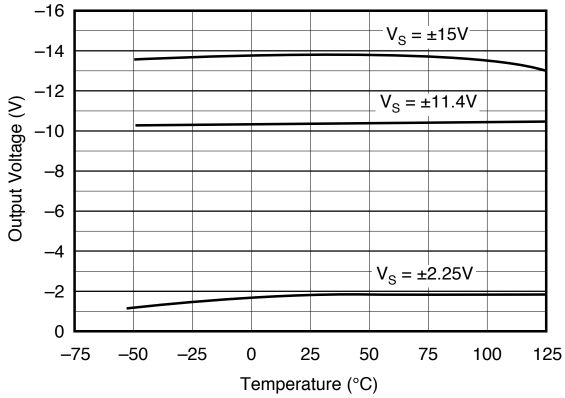
QUIESCENT CURRENT AND POWER DISSIPATION vs POWER SUPPLY VOLTAGE



POSITIVE SIGNAL SWING vs TEMPERATUE ($R_L = 2kΩ$)



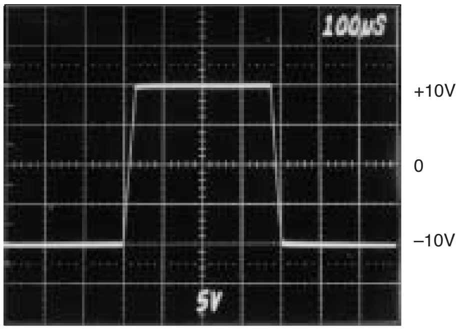
NEGATIVE SIGNAL SWING vs TEMPERATUE ($R_L = 2kΩ$)



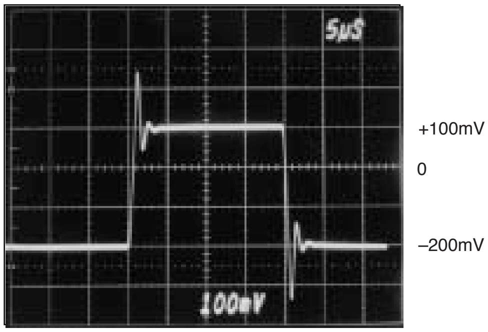
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

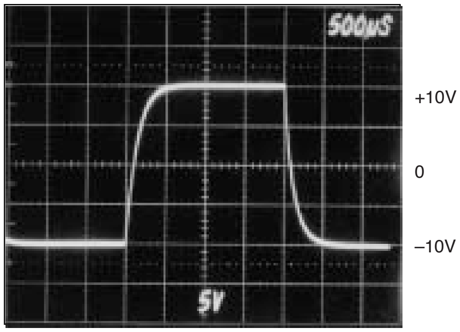
LARGE SIGNAL RESPONSE, G = 1



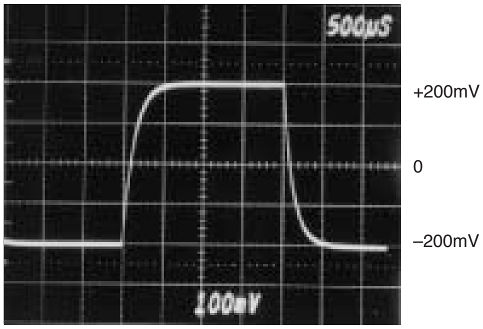
SMALL SIGNAL RESPONSE, G = 1



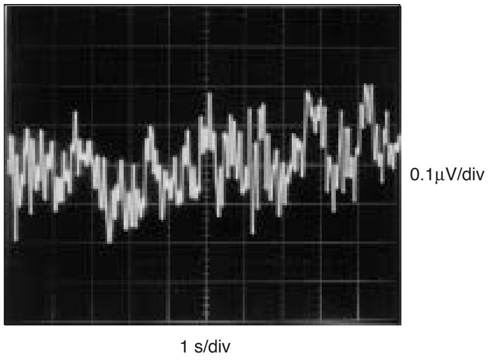
LARGE SIGNAL RESPONSE, G = 1000



SMALL SIGNAL RESPONSE, G = 1000



INPUT-REFERRED NOISE, 0.1 to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA114. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA114 is set by connecting a single external resistor, R_G:

$$G = 1 + \frac{50\ \text{k}\Omega}{R_G} \qquad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

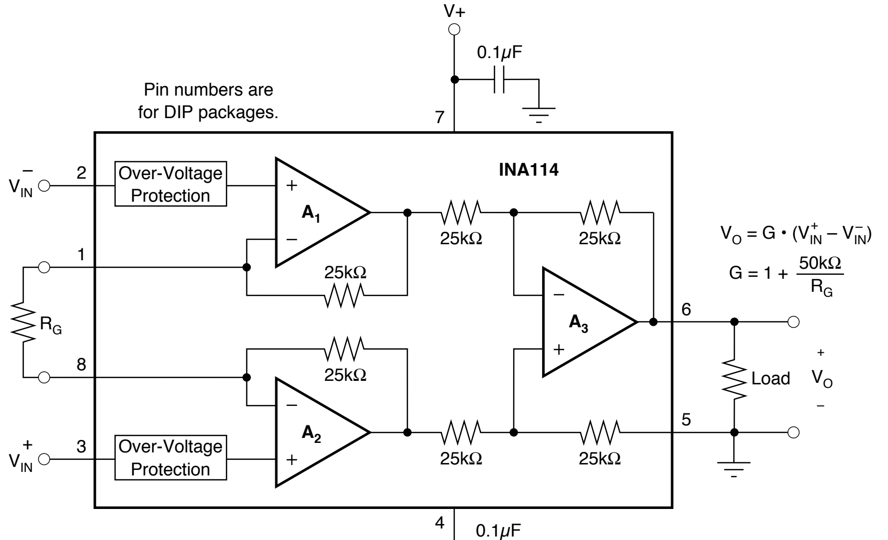
The 50kΩ term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA114.

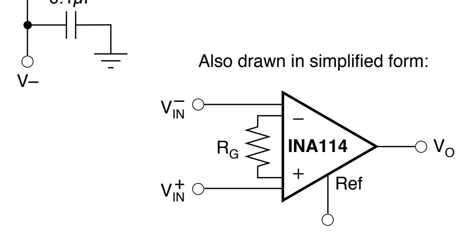
The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

NOISE PERFORMANCE

The INA114 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-input instrumentation amplifier may provide lower noise.

Low frequency noise of the INA114 is approximately 0.4µVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.





DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	No Connection	No Connection
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA114 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

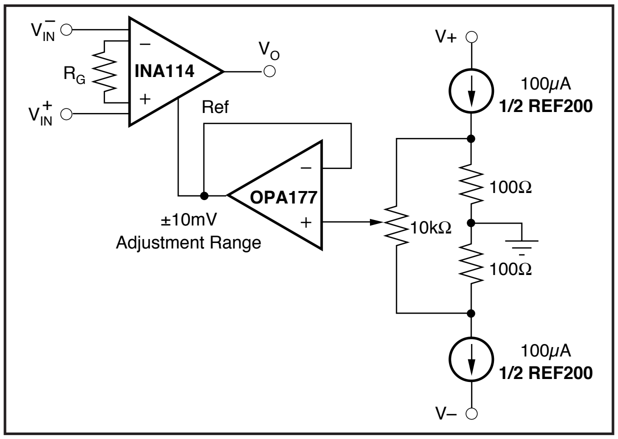


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA114 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA114 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA114 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA114 is approximately ±13.75V (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage."

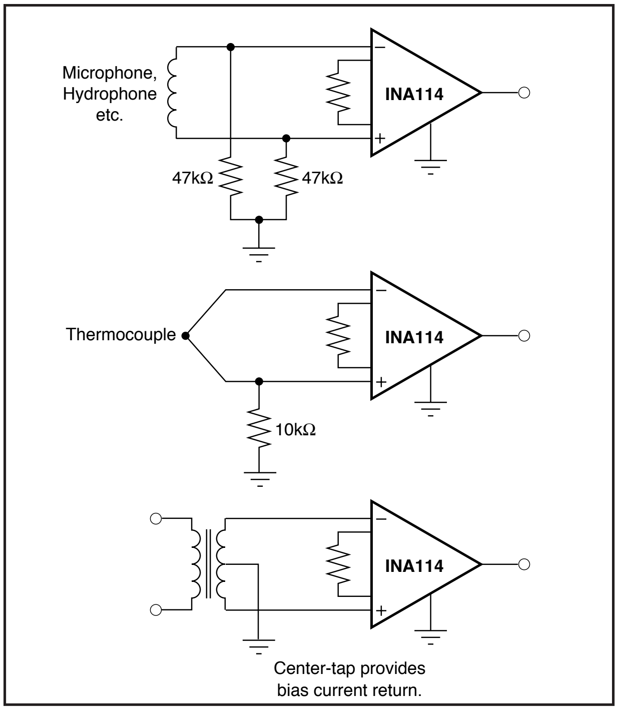


FIGURE 3. Providing an Input Common-Mode Current Path.

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA114 in a lower gain (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the INA114 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA114 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA114 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

OUTPUT VOLTAGE SENSE (SOL-16 package only)

The surface-mount version of the INA114 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA114.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. Figure 5 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1. Heavy loads or long lines can be driven by connecting a buffer inside the feedback path (Figure 6).

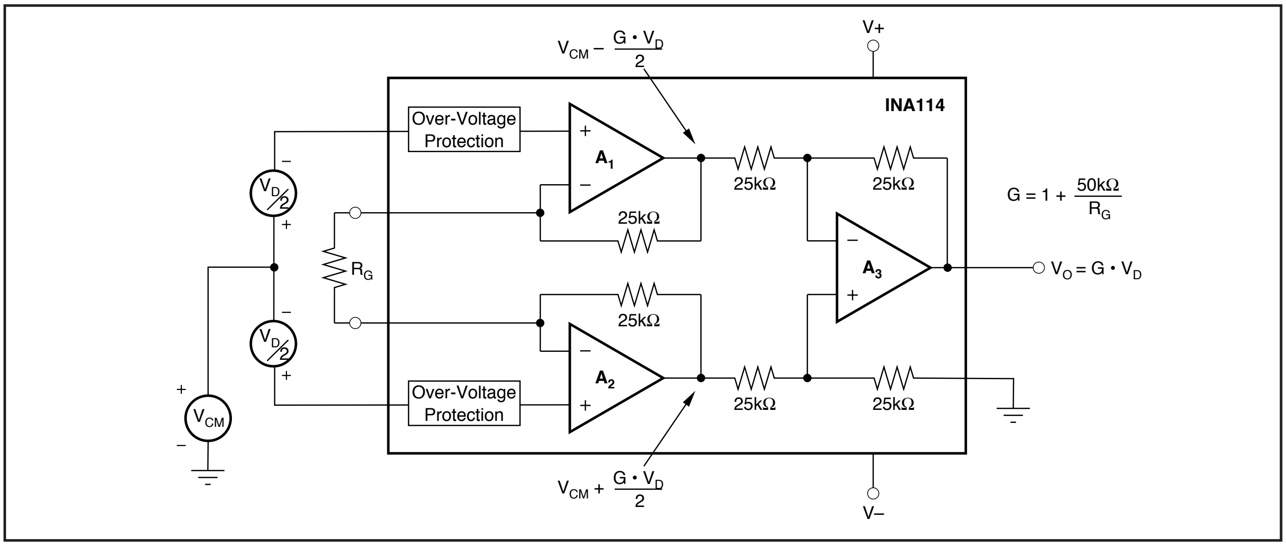
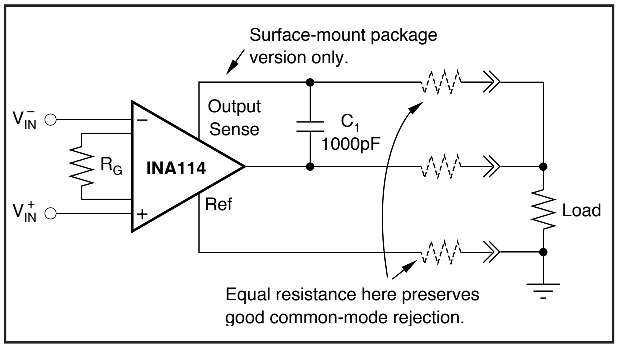


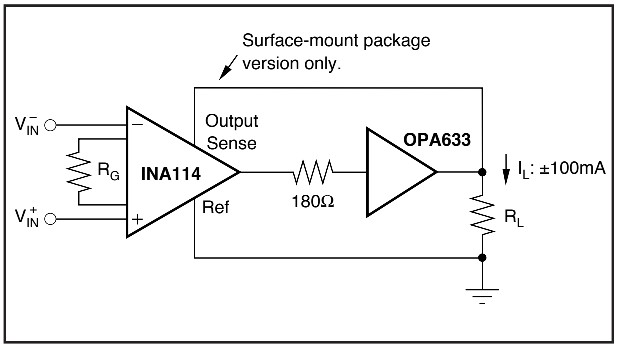
FIGURE 4. Voltage Swing of A_1 and A_2.



Surface-mount package version only.

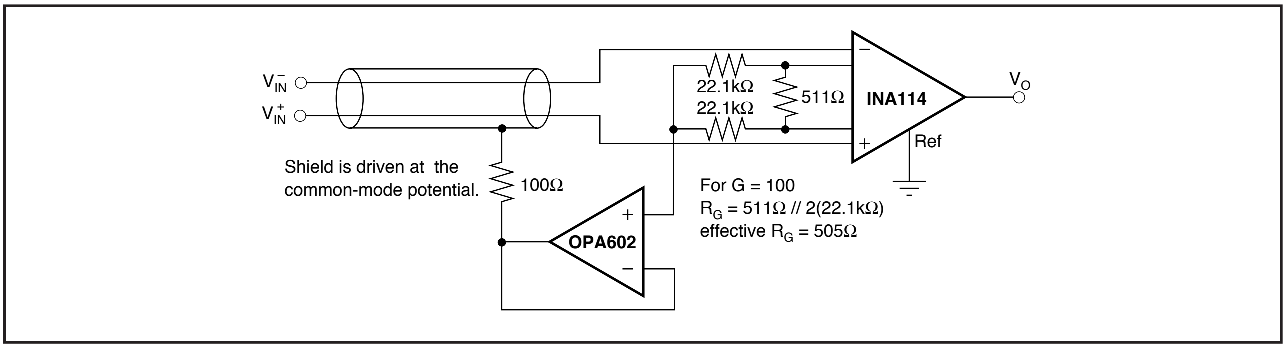
Equal resistance here preserves good common-mode rejection.

FIGURE 5. Remote Load and Ground Sensing.



Surface-mount package version only.

FIGURE 6. Buffered Output for Heavy Loads.



Shield is driven at the common-mode potential.

For G = 100
$R_G = 511\Omega \,//\, 2(22.1k\Omega)$
effective $R_G = 505\Omega$

FIGURE 7. Shield Driver Circuit.

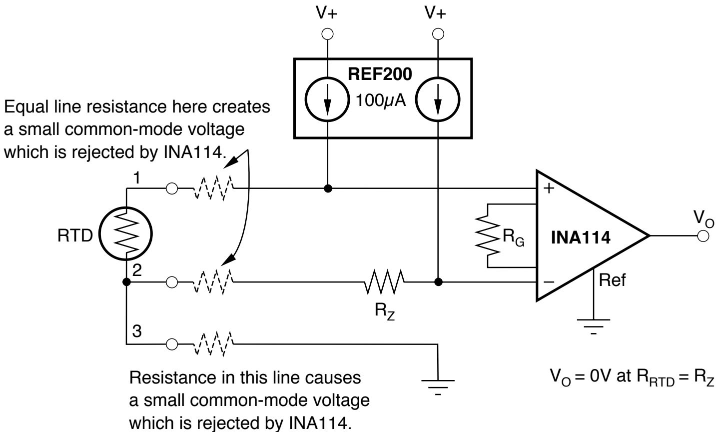
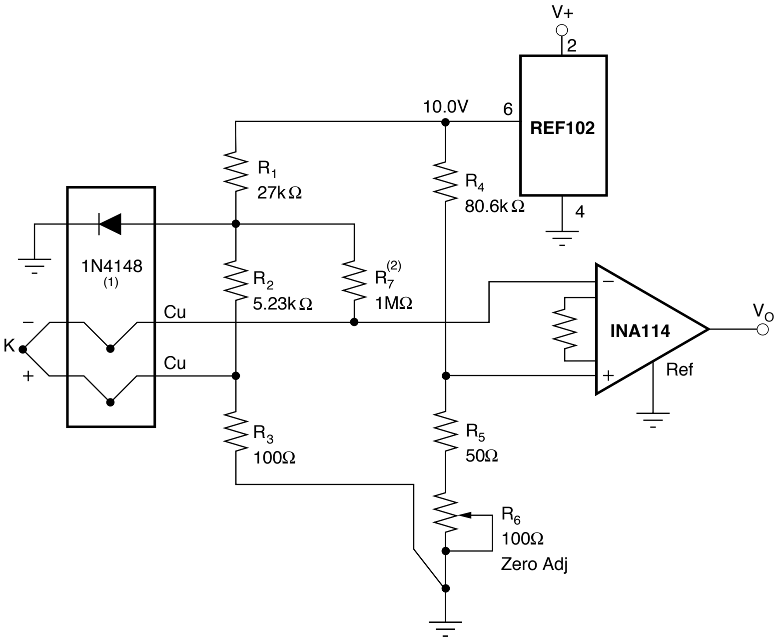


FIGURE 8. RTD Temperature Measurement Circuit.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R_2 ($R_3 = 100\Omega$)	R_4 ($R_5 + R_6 = 100\Omega$)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

NOTES: (1) –2.1mV/°C at 200μA. (2) R_7 provides down-scale burn-out indication.

FIGURE 9. Thermocouple Amplifier With Cold Junction Compensation.

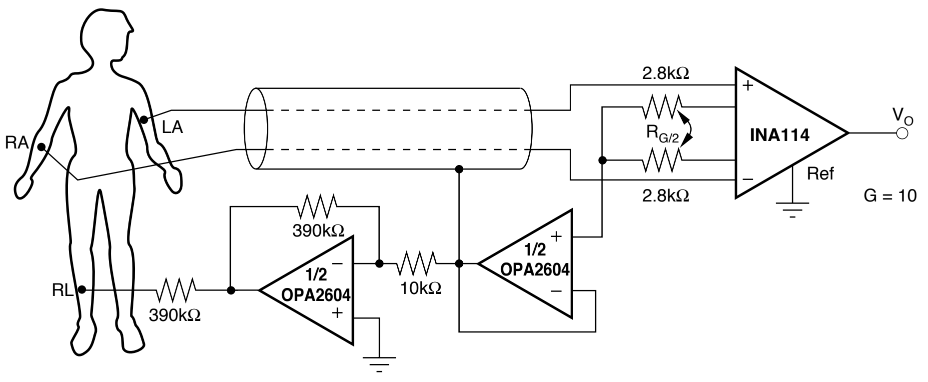


FIGURE 10. ECG Amplifier With Right-Leg Drive.

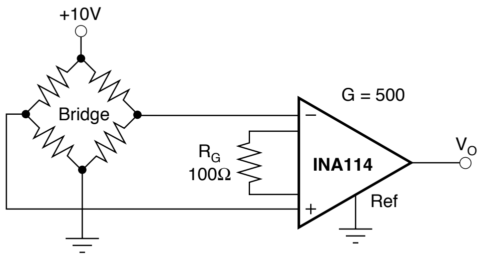


FIGURE 11. Bridge Transducer Amplifier.

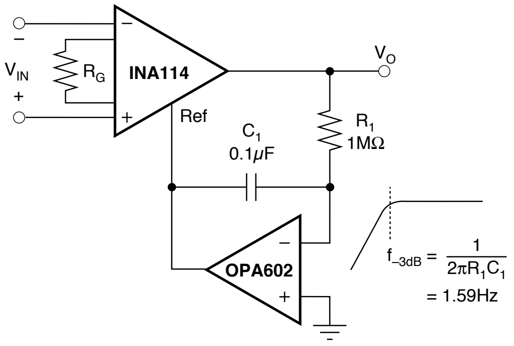
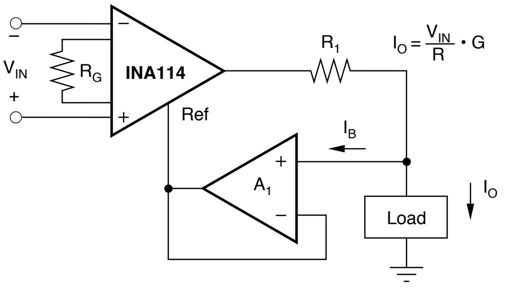


FIGURE 12. AC-Coupled Instrumentation Amplifier.



A_1	I_B Error
OPA177	±1.5nA
OPA602	1pA
OPA128	75fA

FIGURE 13. Differential Voltage-to-Current Converter.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
INA114AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA114APG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA114AU	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA114AU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA114AU/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA114AUE4	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA114AUG4	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA114BP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA114BPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA114BU	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA114BU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA114BU/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA114BUE4	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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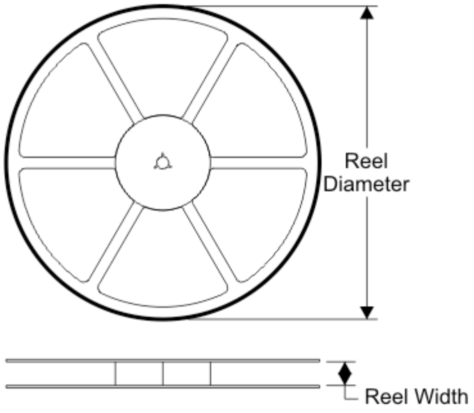
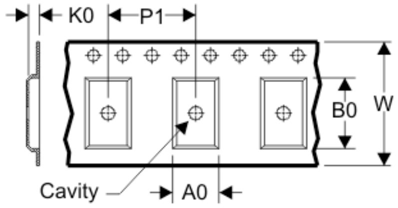
TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

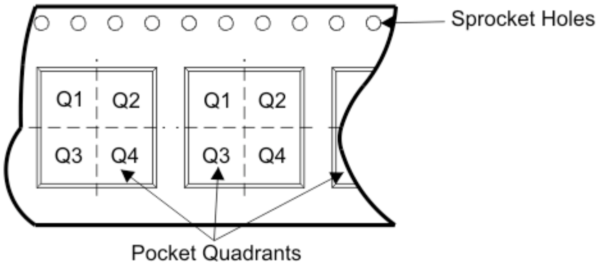


TAPE DIMENSIONS



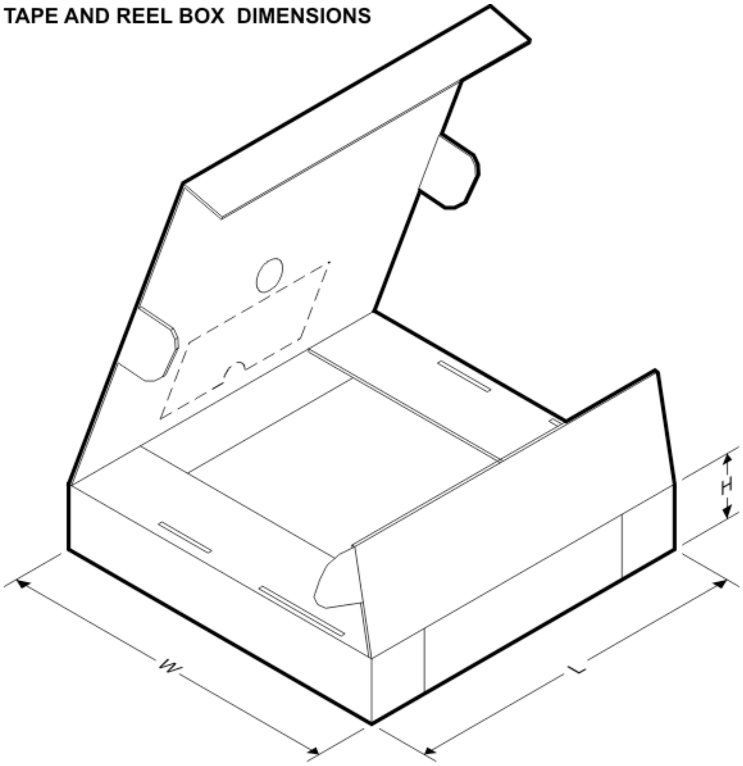
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA114BU/1K	DW	16	SITE 41	330	16	10.85	10.8	2.7	12	16	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
INA114BU/1K	DW	16	SITE 41	346.0	346.0	33.0

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TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080J – SEPTEMBER 1978 – REVISED MARCH 2005

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **Low Noise**
  $V_n = 18\ \text{nV}/\sqrt{\text{Hz}}$ Typ at f = 1 kHz
- **High Input Impedance . . . JFET Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

description/ordering information

The JFET-input operational amplifiers in the TL07x series are similar to the TL08x series, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07x series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

description/ordering information (continued)

ORDERING INFORMATION

T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	10 mV	PDIP (P)	Tube of 50	TL071CP	TL071CP
			Tube of 50	TL072CP	TL072CP
		PDIP (N)	Tube of 25	TL074CN	TL074CN
		SOIC (D)	Tube of 75	TL071CD	TL071C
			Reel of 2500	TL071CDR	
			Tube of 75	TL072CD	TL072C
			Reel of 2500	TL072CDR	
			Tube of 50	TL074CD	TL074C
			Reel of 2500	TL074CDR	
		SOP (NS)	Reel of 2000	TL074CNSR	TL074
		SOP (PS)	Reel of 2000	TL071CPSR	TL071
			Reel of 2000	TL072CPSR	T072
		TSSOP (PW)	Reel of 2000	TL072CPWR	T072
			Tube of 90	TL074CPW	T074
			Reel of 2000	TL074CPWR	
	6 mV	PDIP (P)	Tube of 50	TL071ACP	TL071ACP
			Tube of 50	TL072ACP	TL072ACP
		PDIP (N)	Tube of 25	TL074ACN	TL074ACN
		SOIC (D)	Tube of 75	TL071ACD	071AC
			Reel of 2500	TL071ACDR	
			Tube of 75	TL072ACD	072AC
			Reel of 2500	TL072ACDR	
			Tube of 50	TL074ACD	TL074AC
			Reel of 2500	TL074ACDR	
		SOP (PS)	Reel of 2000	TL072ACPSR	T072A
		SOP (NS)	Reel of 2000	TL074ACNSR	TL074A
	3 mV	PDIP (P)	Tube of 50	TL071BCP	TL071BCP
			Tube of 50	TL072BCP	TL072BCP
		PDIP (N)	Tube of 25	TL074BCN	TL074BCN
		SOIC (D)	Tube of 75	TL071BCD	071BC
			Reel of 2500	TL071BCDR	
			Tube of 75	TL072BCD	072BC
			Reel of 2500	TL072BCDR	
			Tube of 50	TL074BCD	TL074BC
			Reel of 2500	TL074BCDR	
		SOP (NS)	Reel of 2000	TL074BCNSR	TL074B

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

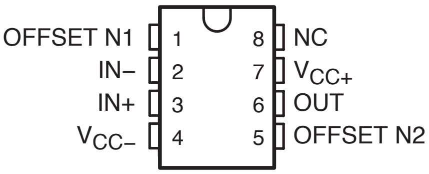
description/ordering information (continued)

ORDERING INFORMATION

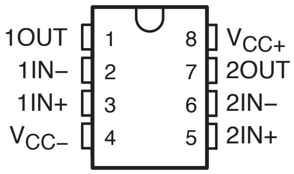
T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL071IP	TL071IP
			Tube of 50	TL072IP	TL072IP
		PDIP (N)	Tube of 25	TL074IN	TL074IN
		SOIC (D)	Tube of 75	TL071ID	TL071I
			Reel of 2500	TL071IDR	
			Tube of 75	TL072ID	TL072I
			Reel of 2500	TL072IDR	
			Tube of 50	TL074ID	TL074I
			Reel of 2500	TL074IDR	
–55°C to 125°C	6 mV	CDIP (JG)	Tube of 50	TL072MJGB	TL072MJGB
		CFP (U)	Tube of 150	TL072MUB	TL072MUB
		LCCC (FK)	Tube of 55	TL072MFKB	TL072MFKB
	9 mV	CDIP (J)	Tube of 25	TL074MJB	TL074MJB
		CFP (W)	Tube of 25	TL074MWB	TL074MWB
		LCCC (FK)	Tube of 55	TL074MFKB	TL074MFKB

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

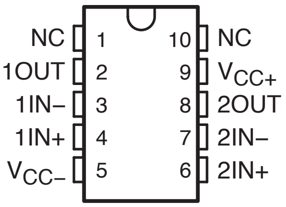
TL071, TL071A, TL071B
D, P, OR PS PACKAGE
(TOP VIEW)



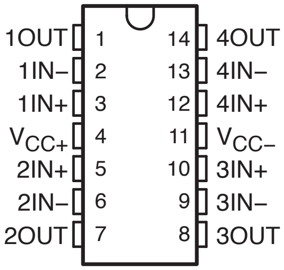
TL072, TL072A, TL072B
D, JG, P, PS, OR PW PACKAGE
(TOP VIEW)



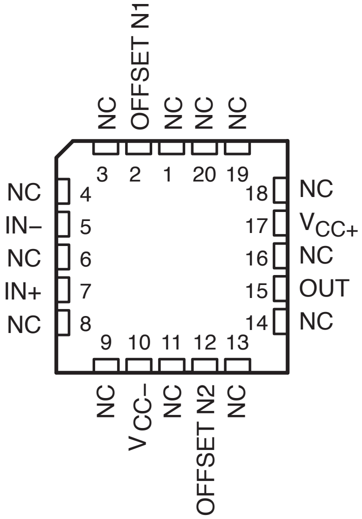
TL072
U PACKAGE
(TOP VIEW)



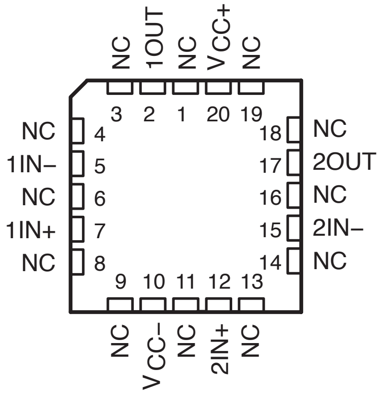
TL074A, TL074B
D, J, N, NS, OR PW PACKAGE
TL074 . . . D, J, N, NS, PW,
OR W PACKAGE
(TOP VIEW)



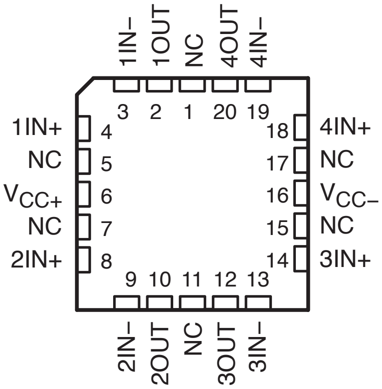
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



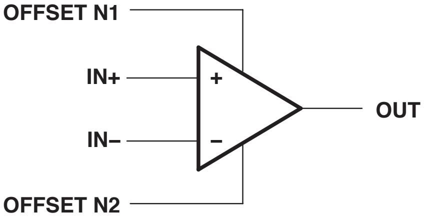
TL074
FK PACKAGE
(TOP VIEW)



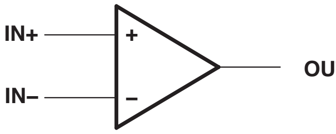
NC – No internal connection

symbols

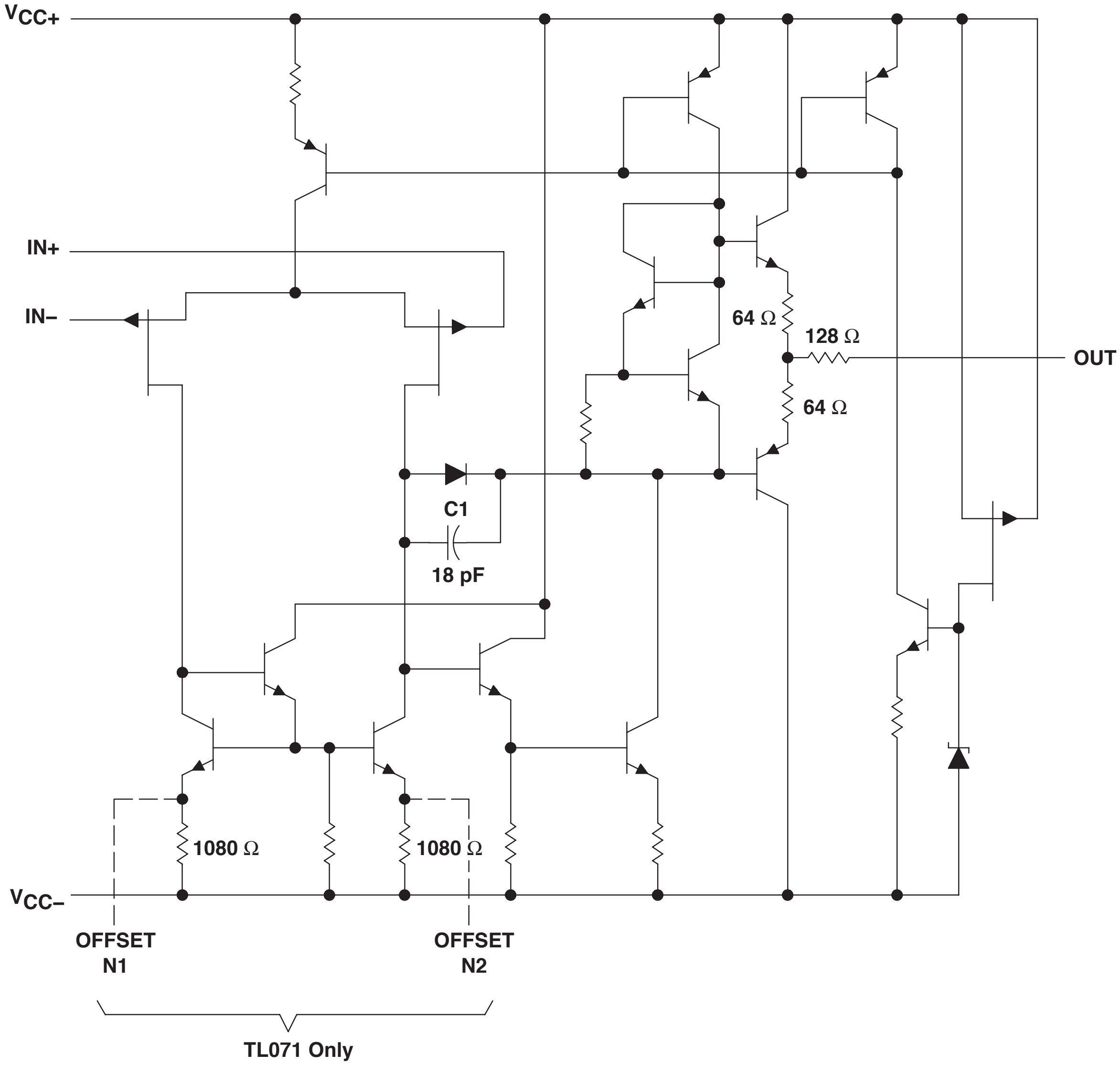
TL071



TL072 (each amplifier)
TL074 (each amplifier)



schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+}		18 V
V_{CC-}		–18 V
Differential input voltage, V_{ID} (see Note 2)		±30 V
Input voltage, V_I (see Notes 1 and 3)		±15 V
Duration of output short circuit (see Note 4)		Unlimited
Package thermal impedance, θ_{JA} (see Notes 5 and 6):	D package (8 pin)	97°C/W
	D package (14 pin)	86°C/W
	N package	80°C/W
	NS package	76°C/W
	P package	85°C/W
	PS package	95°C/W
	PW package (8 pin)	149°C/W
	PW package (14 pin)	113°C/W
	U package	185°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8):	FK package	5.61°C/W
	J package	15.05°C/W
	JG package	14.5°C/W
	W package	14.65°C/W
Operating virtual junction temperature, T_J		150°C
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package		300°C
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+, with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of T_J(max), θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10		3	6		2	3		3	6	mV
			Full range			13			7.5			5			8	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100		5	100		5	100	pA
			Full range			10			2			2			2	nA
I_{IB}	Input bias current§	V_O = 0	25°C		65	200		65	200		65	200		65	200	pA
			Full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		$R_L \geq$ 10 kΩ	Full range	±12			±12			±12			±12			
		$R_L \geq$ 2 kΩ		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω	25°C	70	100		75	100		75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

‡ Full range is T_A = 0°C to 70°C for TL07_C,TL07_AC, TL07_BC and is T_A = −40°C to 85°C for TL07_I.

§ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	6		3	9	mV
			Full range			9			15	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18			18		μV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		±12	±13.5		V
		$R_L \geq 10\ k\Omega$	Full range	±12			±12			
		$R_L \geq 2\ k\Omega$		±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{min}$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

† Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = −55°C to 125°C.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	5	13		8	13		V/µs
t_r	Rise-time overshoot factor	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		µs
					20%			20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		µV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	V_Irms = 6 V, R_L ≥ 2 kΩ, f = 1 kHz	A_{VD} = 1, R_S ≤ 1 kΩ,		0.003 %			0.003%		

PARAMETER MEASUREMENT INFORMATION

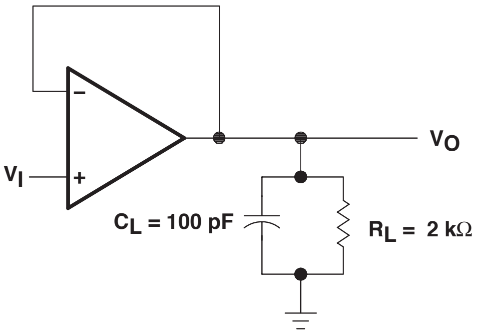


Figure 1. Unity-Gain Amplifier

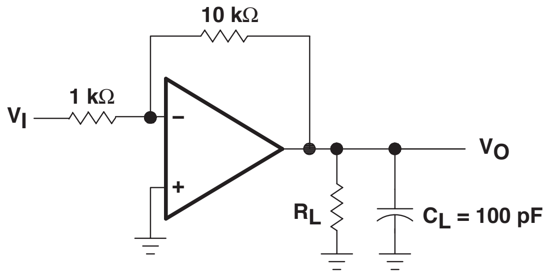


Figure 2. Gain-of-10 Inverting Amplifier

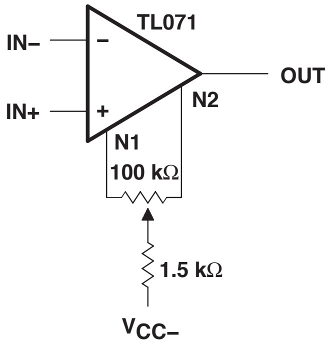


Figure 3. Input Offset-Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	4
V_{OM}	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
CMRR	Common-mode rejection ratio	vs Free-air temperature	14
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	15 16
P_D	Total power dissipation	vs Free-air temperature	17
	Normalized slew rate	vs Free-air temperature	18
V_n	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
	Large-signal pulse response	vs Time	21
V_O	Output voltage	vs Elapsed time	22

TYPICAL CHARACTERISTICS†

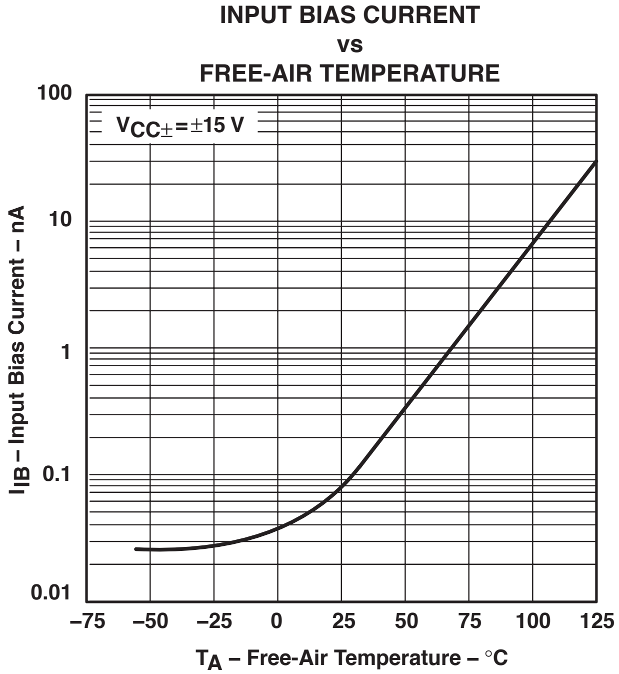


Figure 4

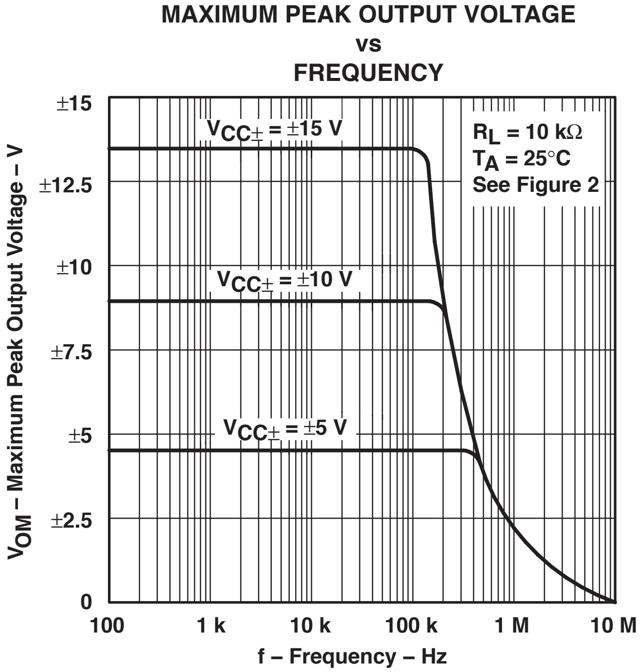


Figure 5

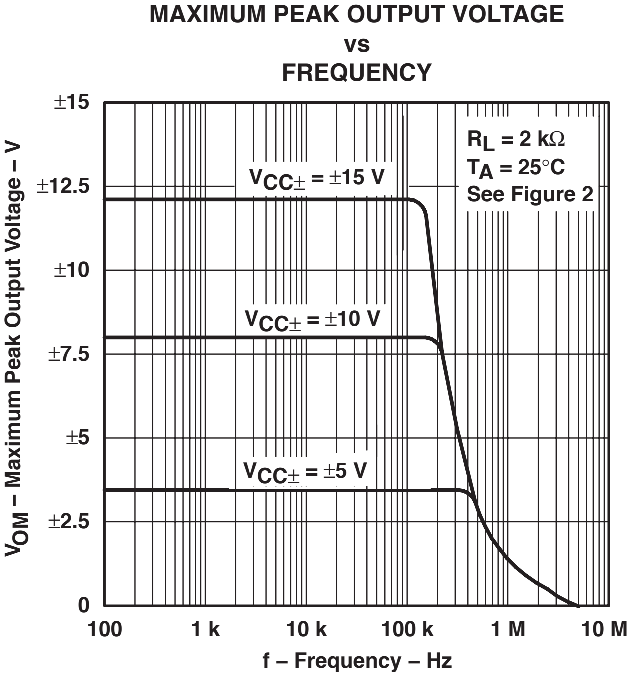


Figure 6

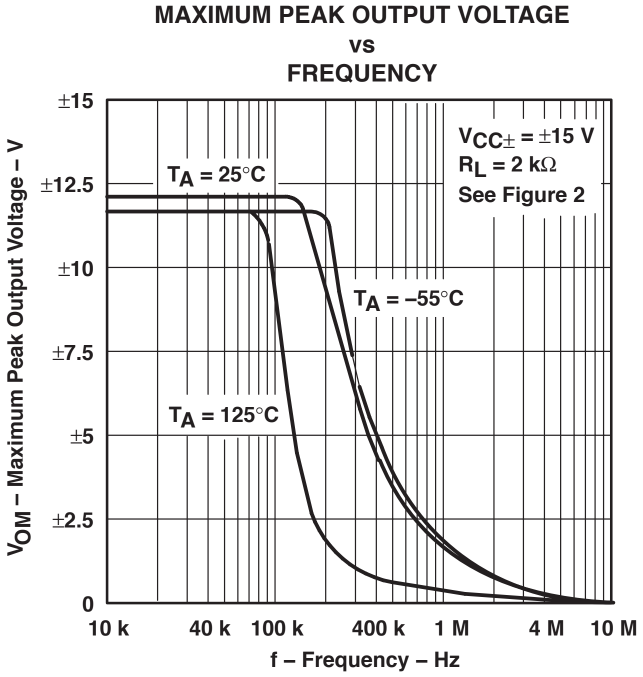


Figure 7

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

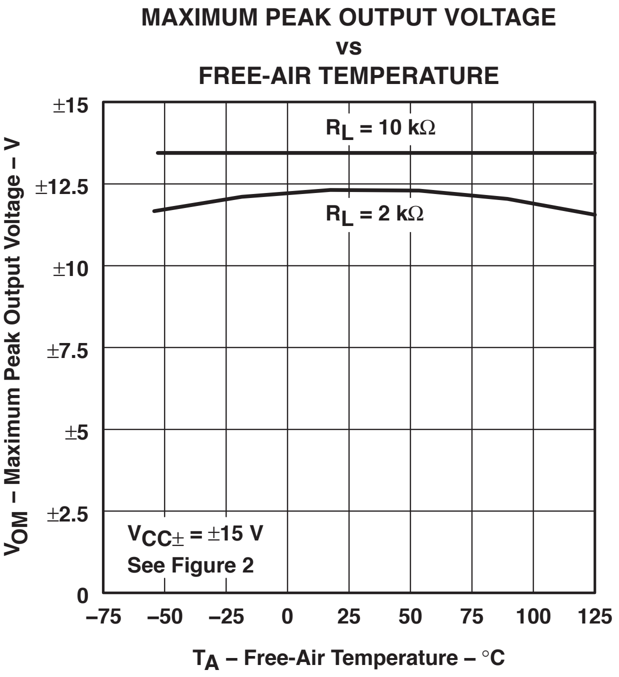

Figure 8

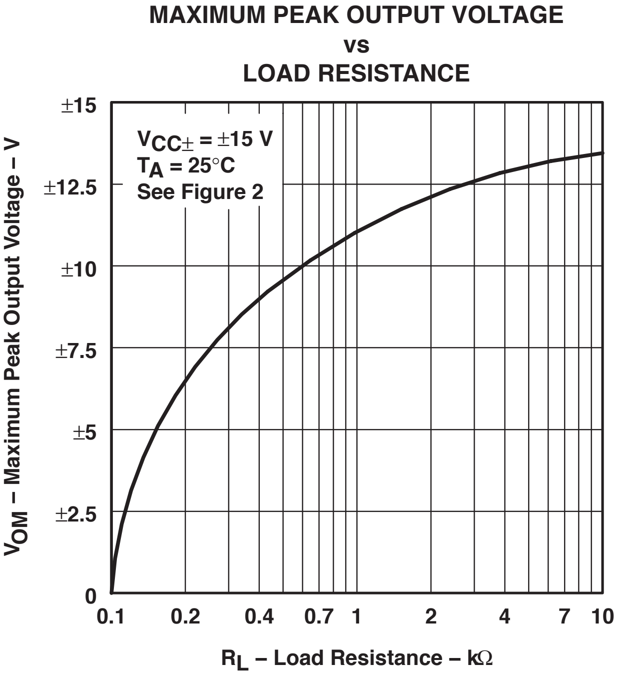

Figure 9

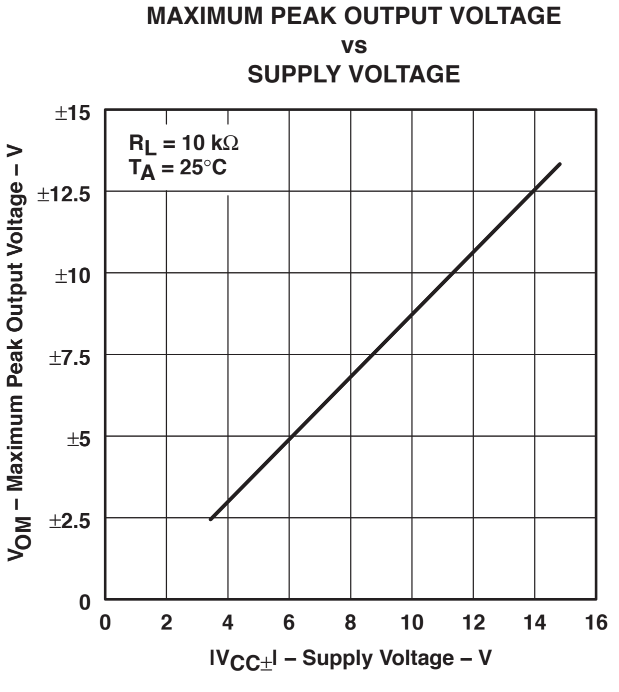

Figure 10

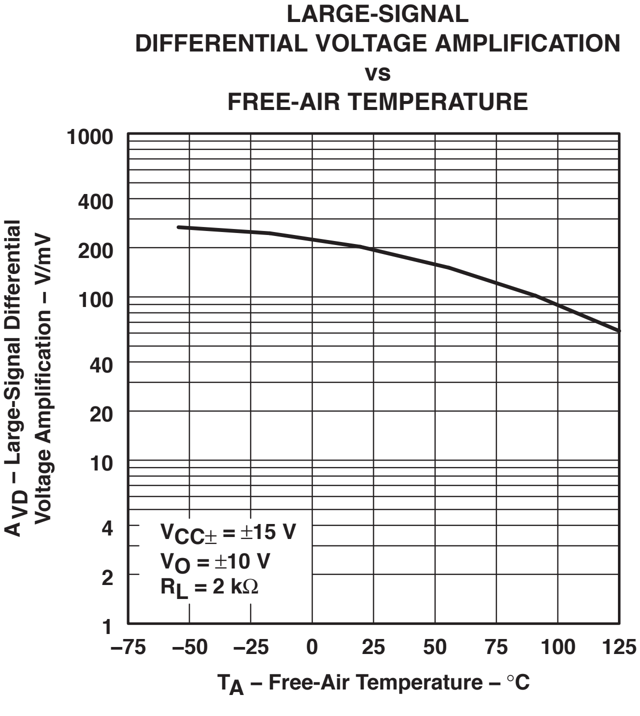

Figure 11

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

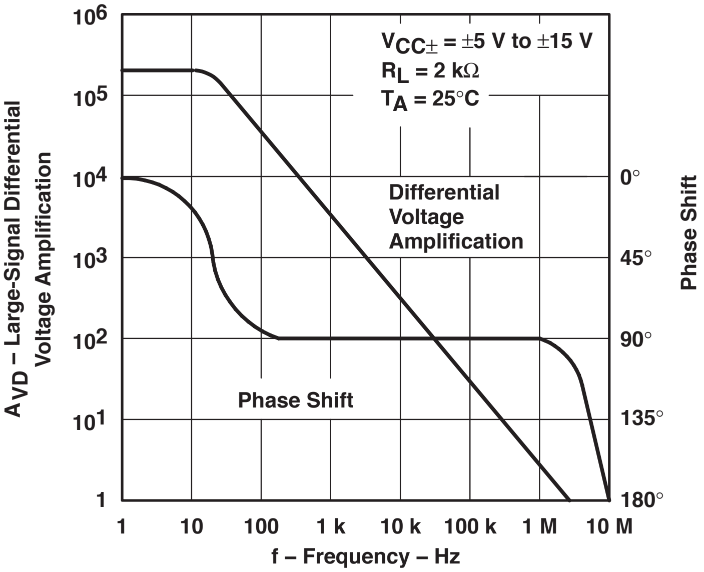

Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE

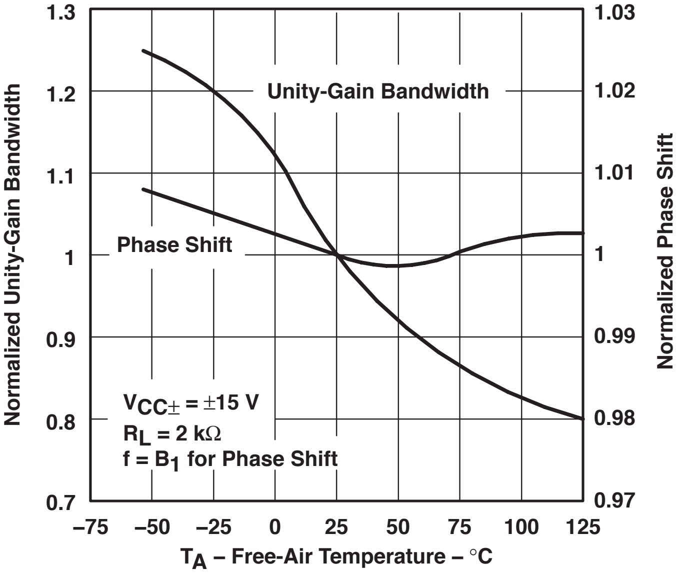

Figure 13

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

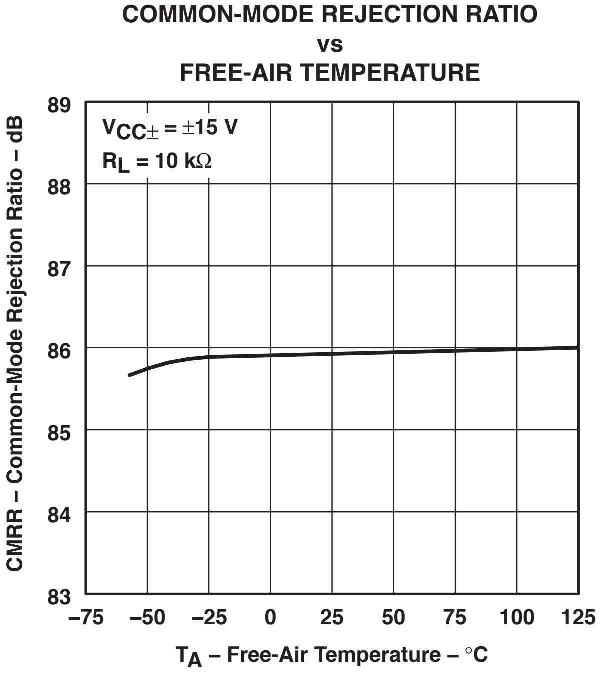

Figure 14

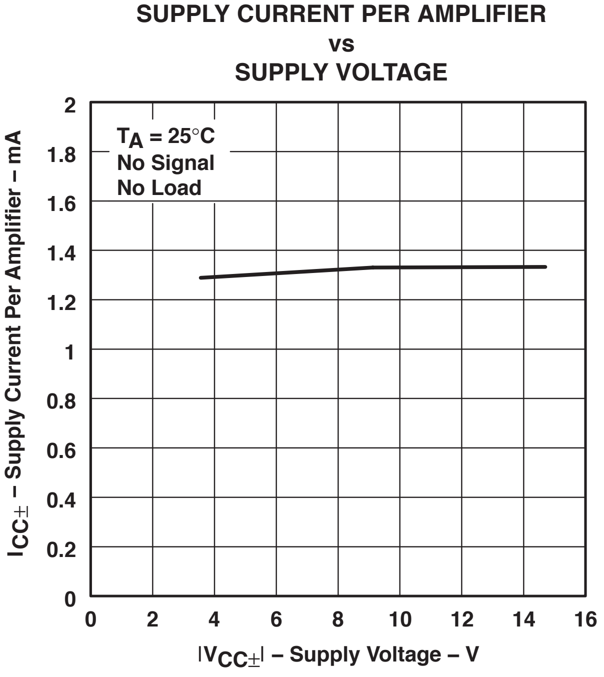

Figure 15

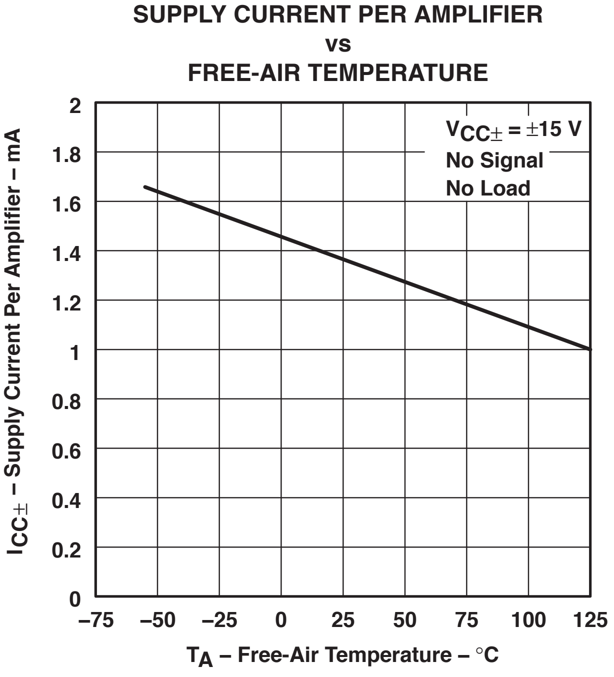

Figure 16

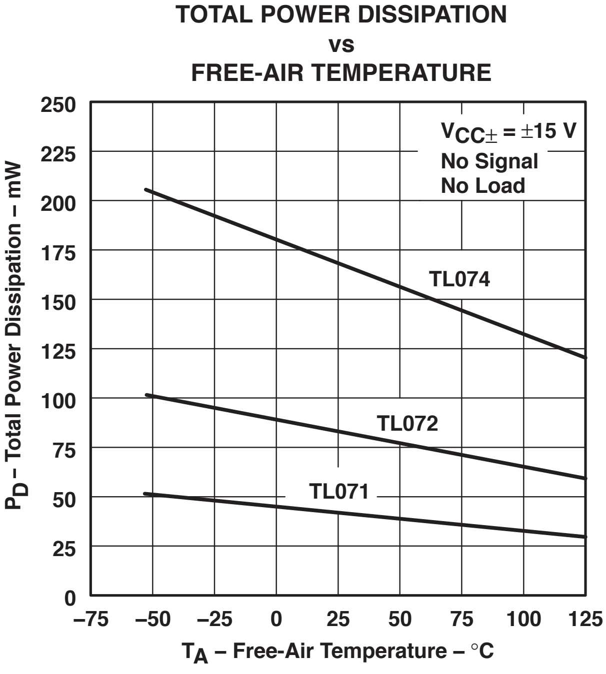

Figure 17

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

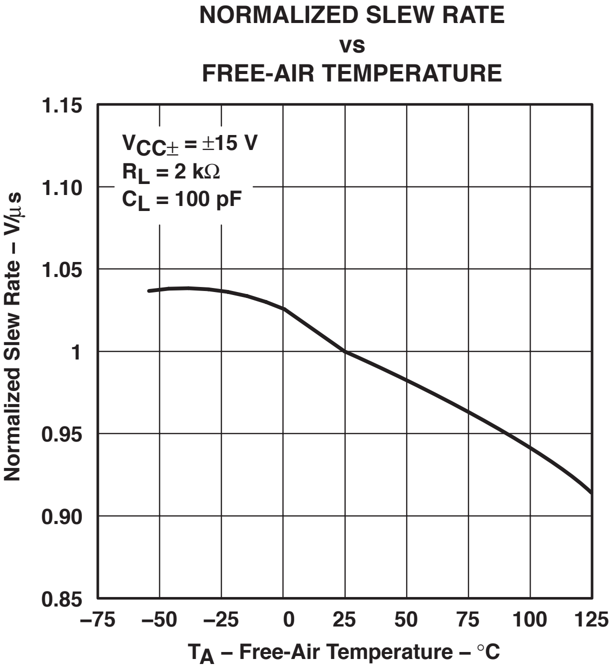


Figure 18

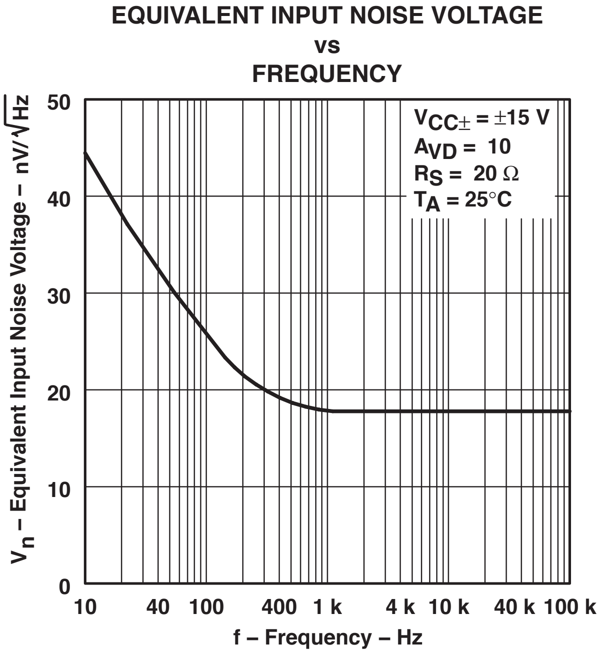


Figure 19

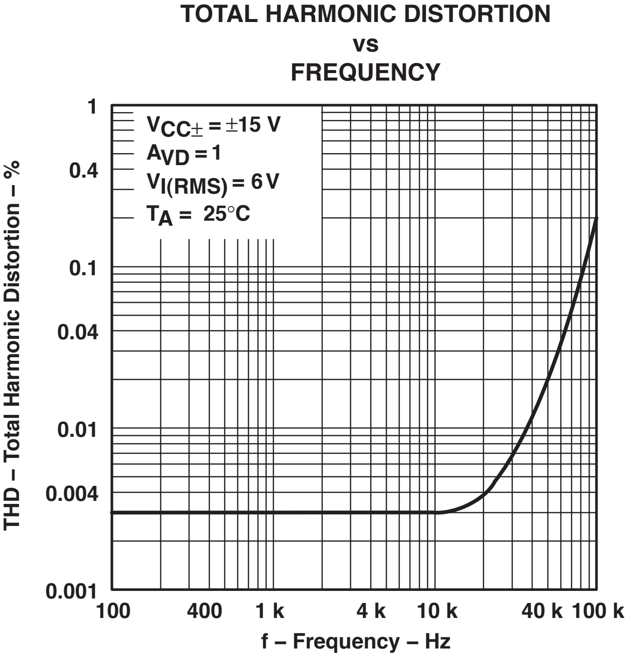


Figure 20

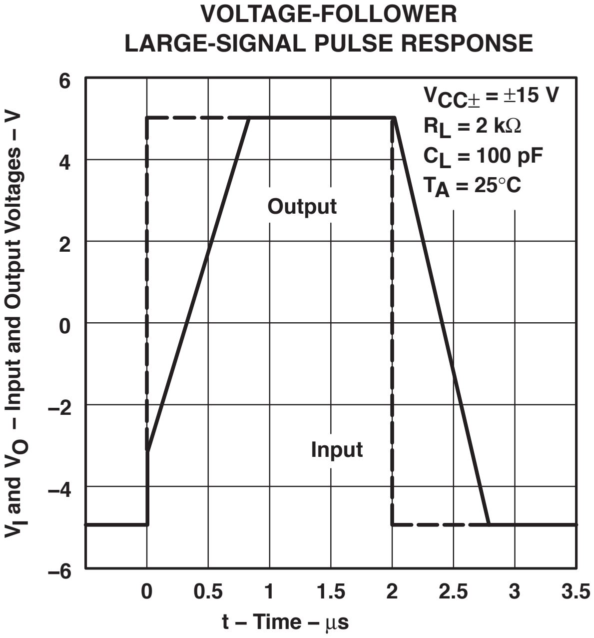


Figure 21

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ELAPSED TIME

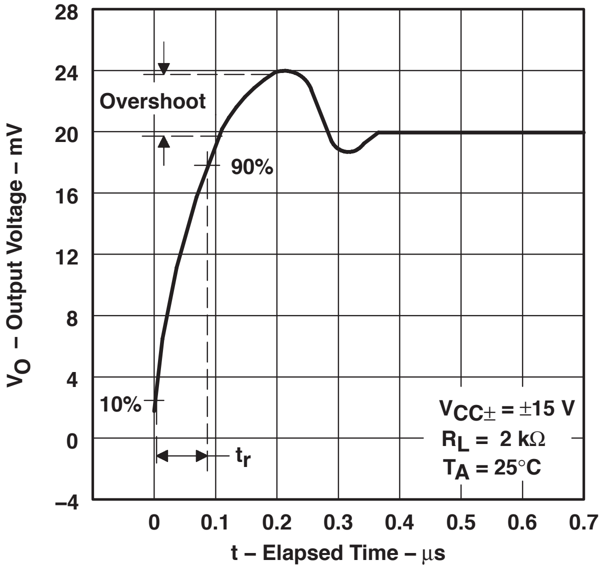


Figure 22

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27

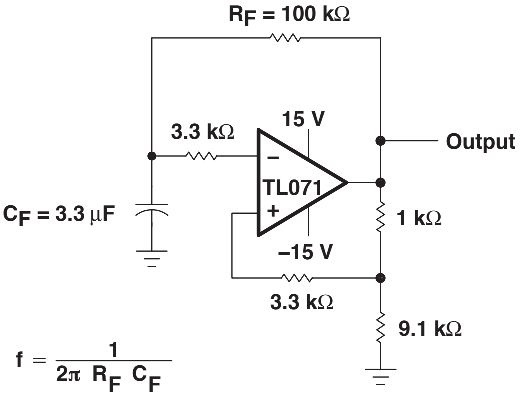


Figure 23. 0.5-Hz Square-Wave Oscillator

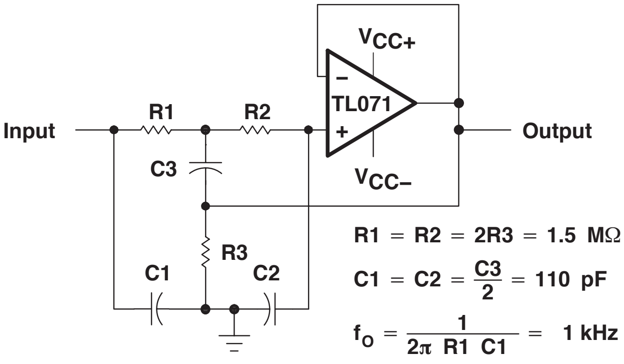


Figure 24. High-Q Notch Filter

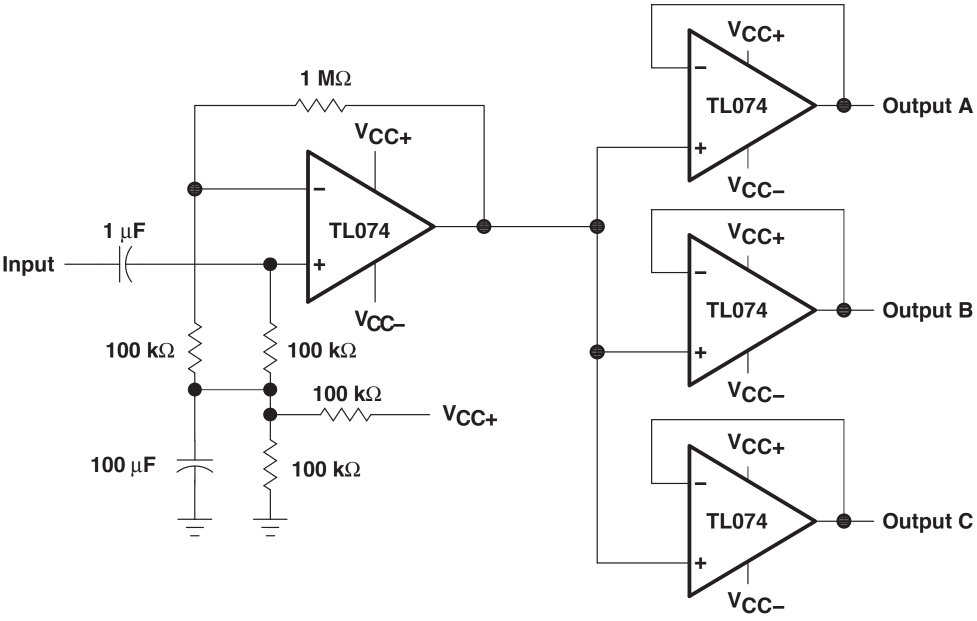
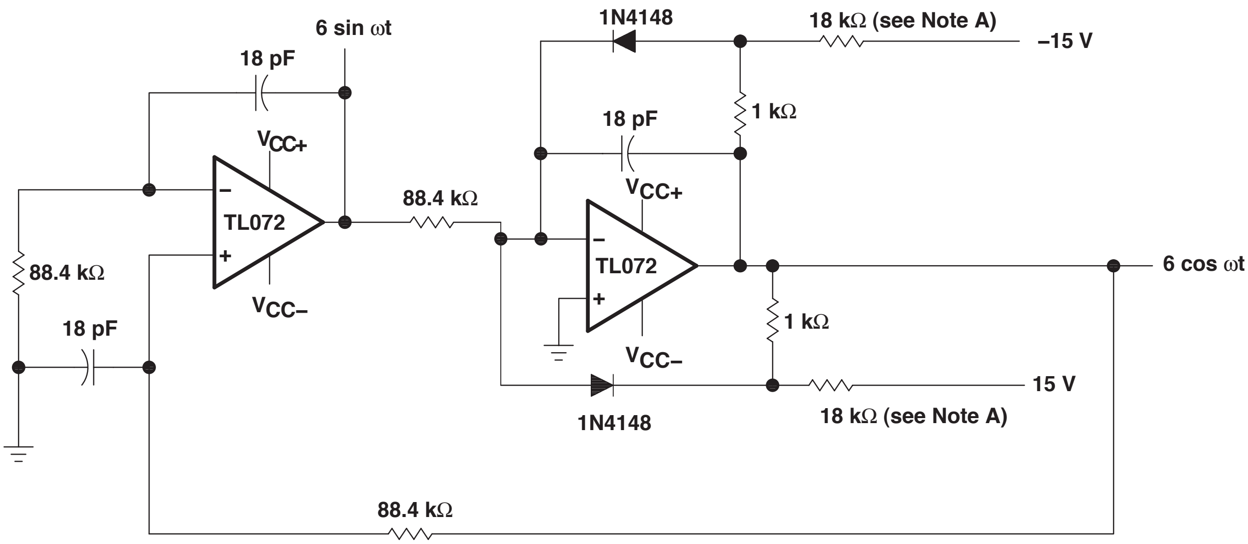


Figure 25. Audio-Distribution Amplifier

APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-kHz Quadrature Oscillator

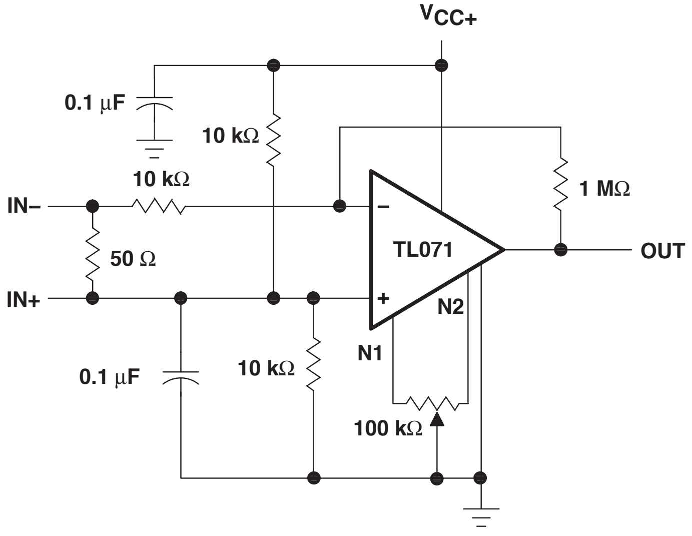


Figure 27. AC Amplifier

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
8102304HA	OBSOLETE			10		TBD	Call TI	Call TI
81023052A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8102305HA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
8102305PA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
81023062A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8102306CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
8102306DA	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/11906BCA	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL071ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL071ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL071BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL071BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL071CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL071CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL071CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
TL071CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TL071ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL071IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL071IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL071MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
TL071MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL071MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL072ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL072ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL072ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL072ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072ACPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL072BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL072CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		
TL072CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL072CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL072CPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI
TL072CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL072IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL072MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TL072MJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TL072MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TL072MUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
TL074ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL074ACJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL074ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL074ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL074ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ACNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL074BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL074BCNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL074CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL074CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074IJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL074IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL074INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL074MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TL074MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TL074MJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
TL074MJB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
TL074MWB	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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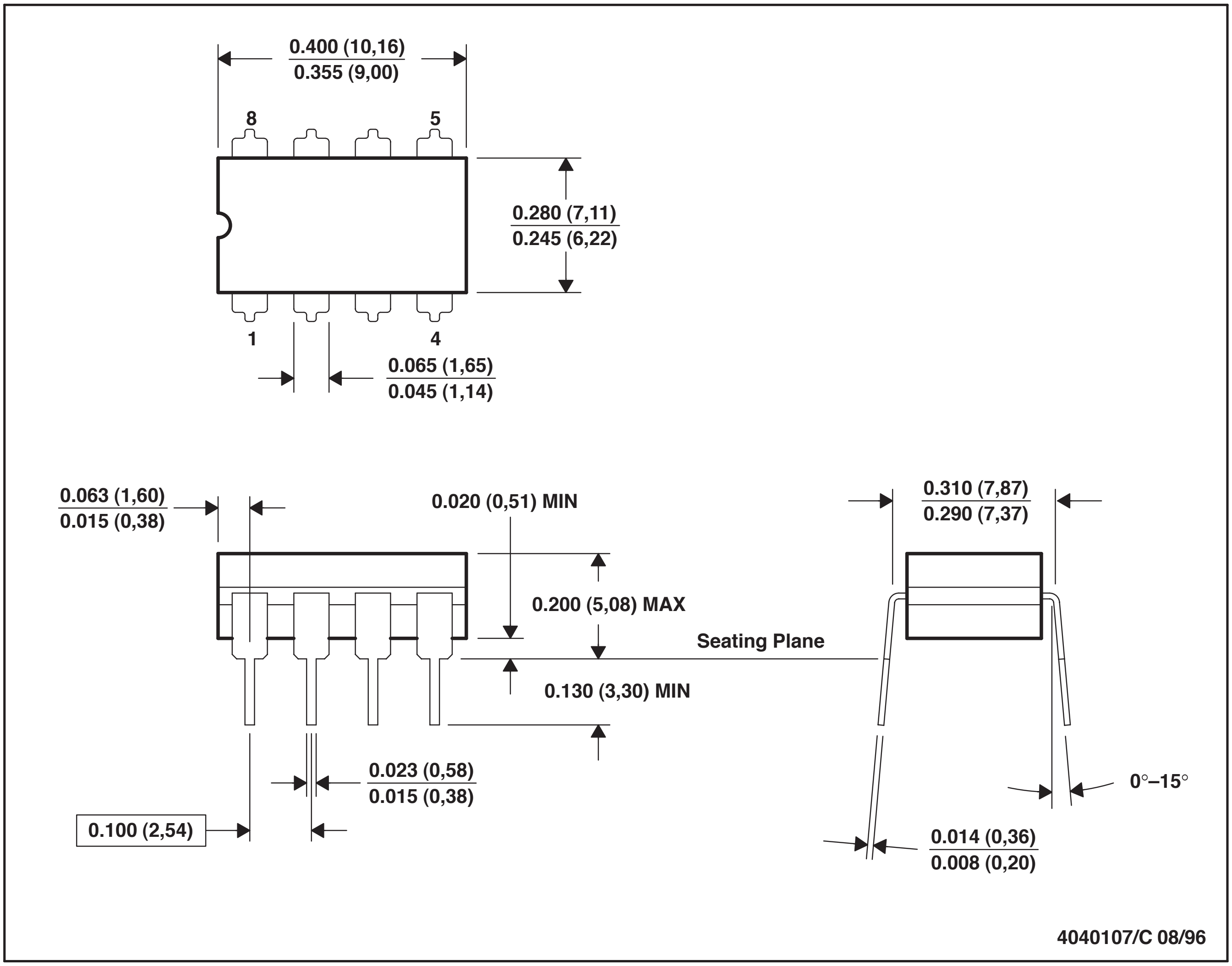
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

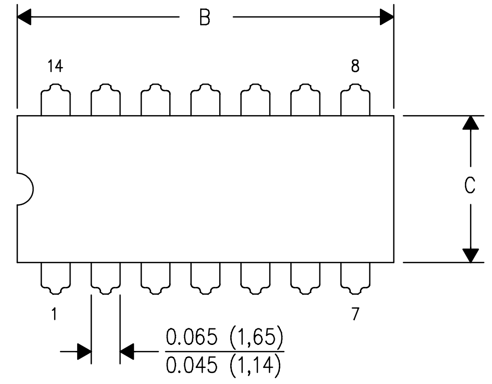
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



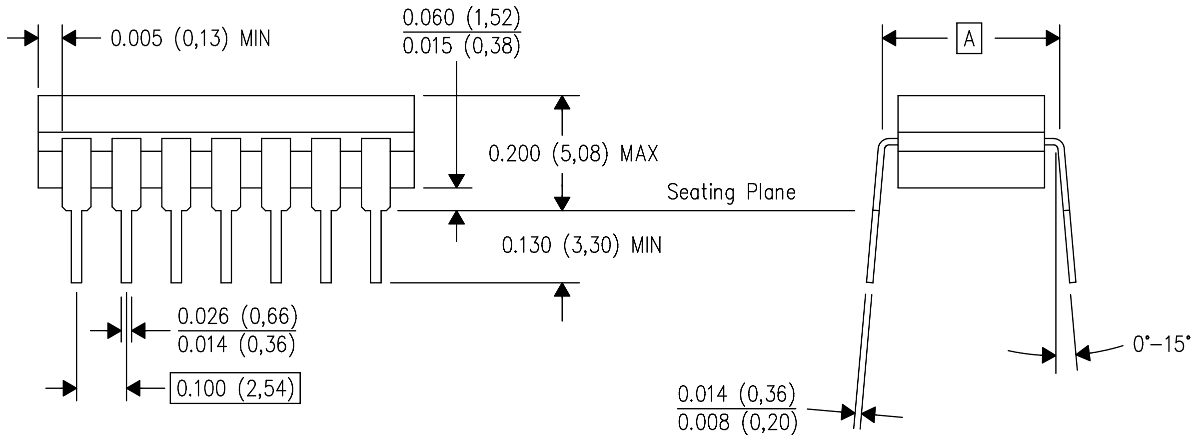
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



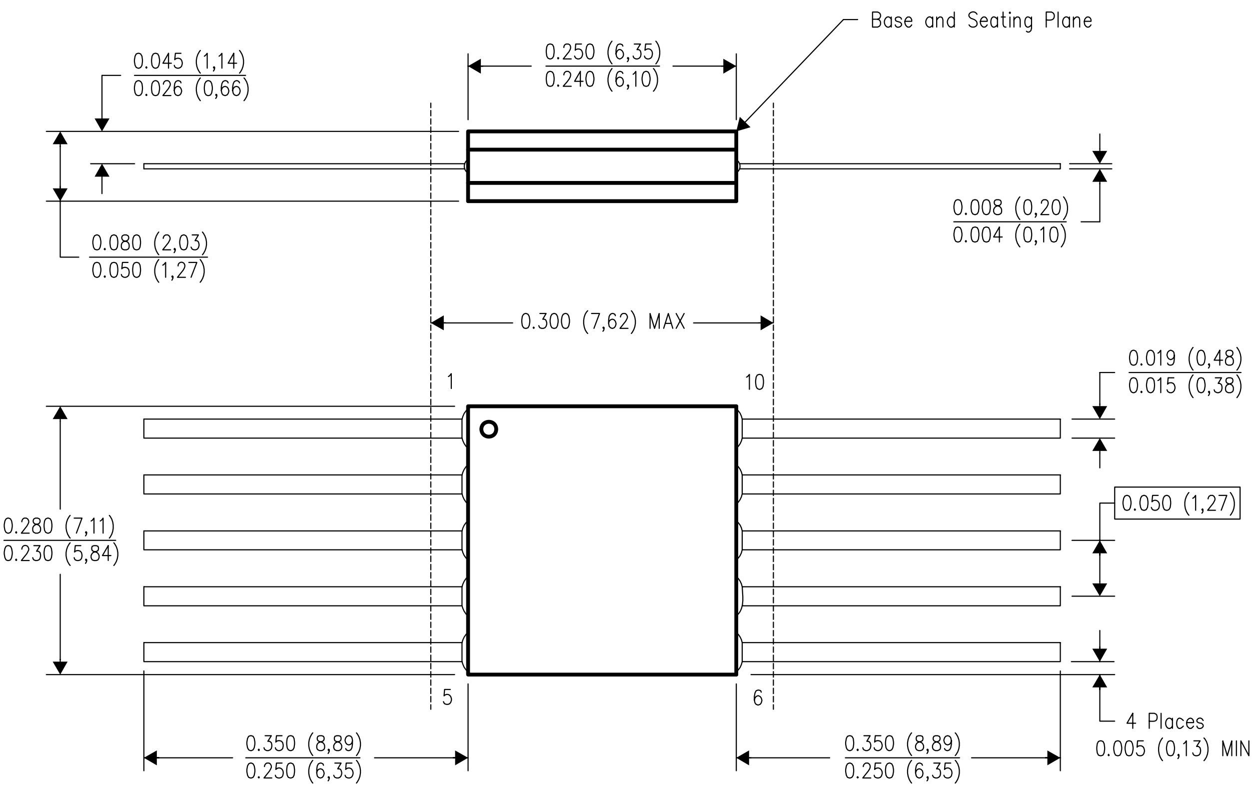
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

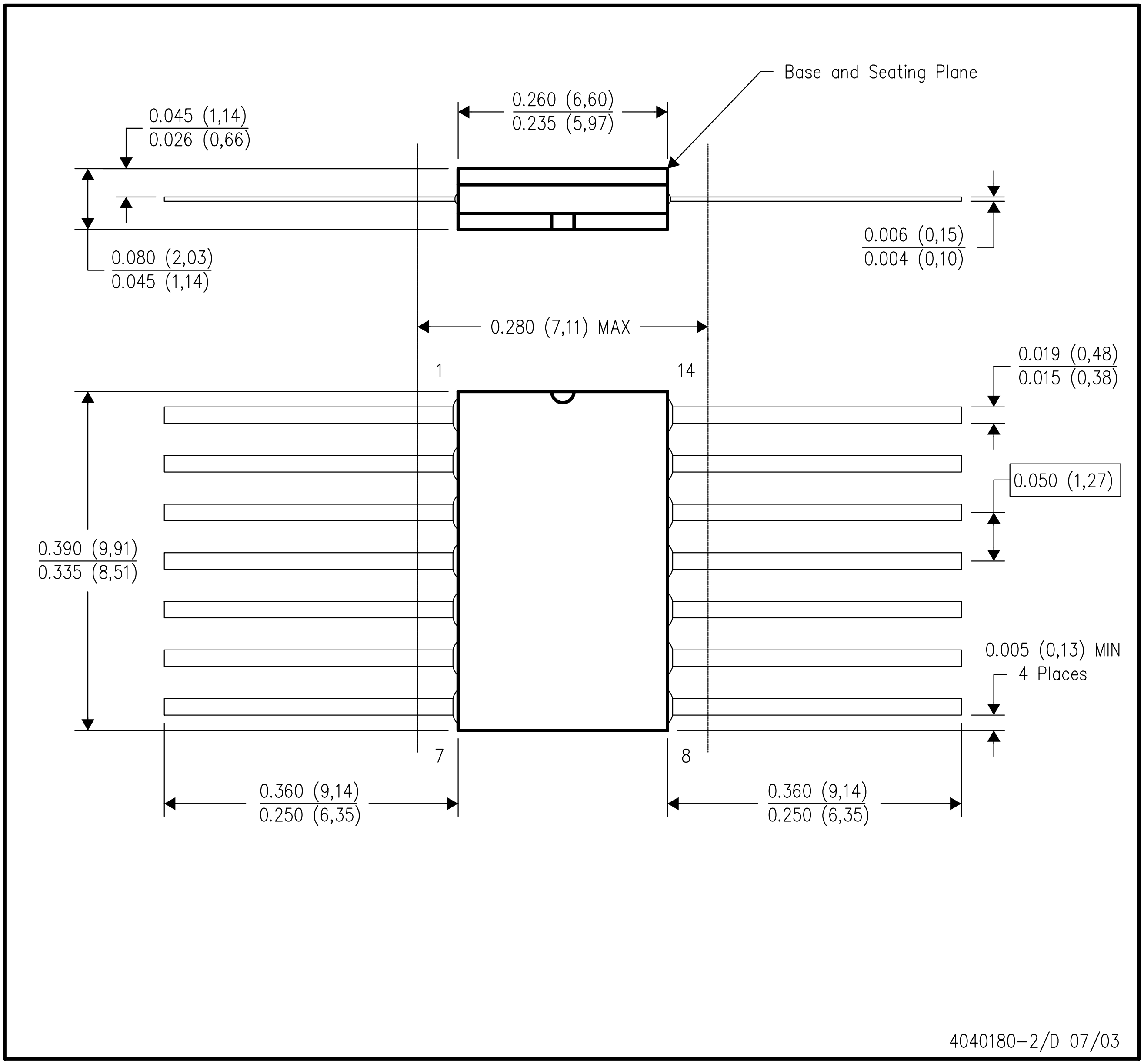
U (S–GDFP–F10) CERAMIC DUAL FLATPACK



4040179/B 03/95

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

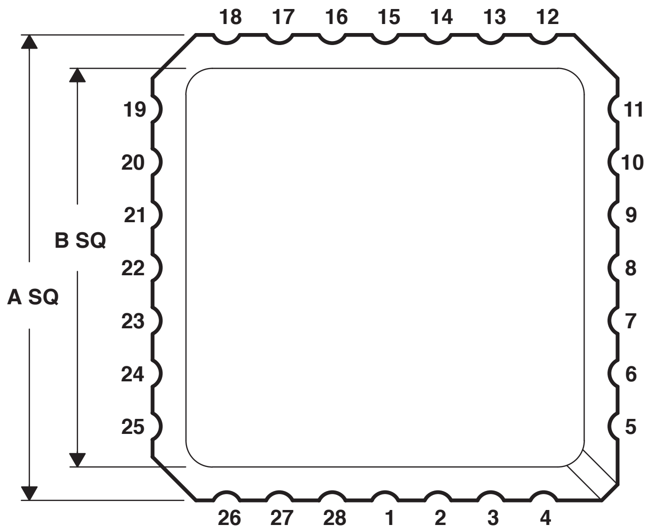
W (R-GDFP-F14) CERAMIC DUAL FLATPACK



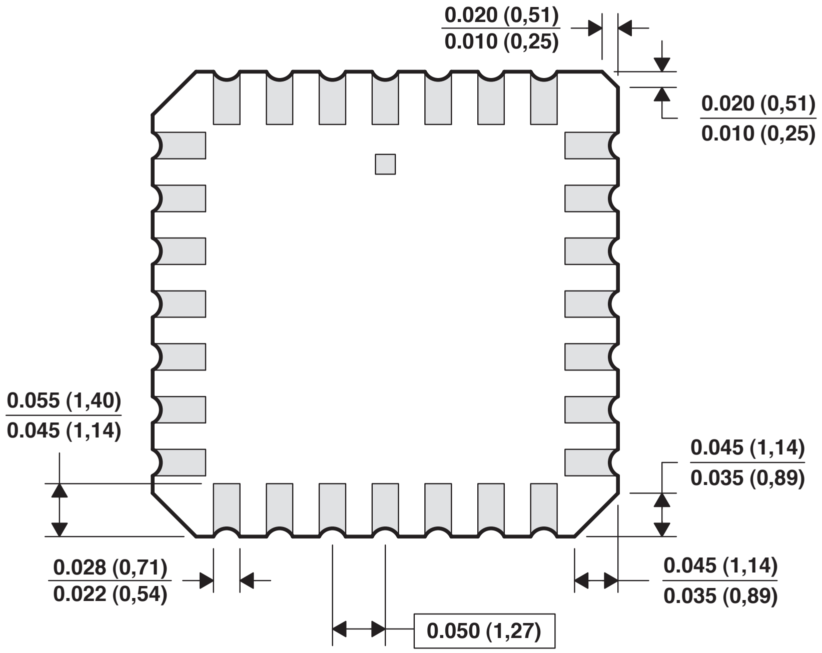
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

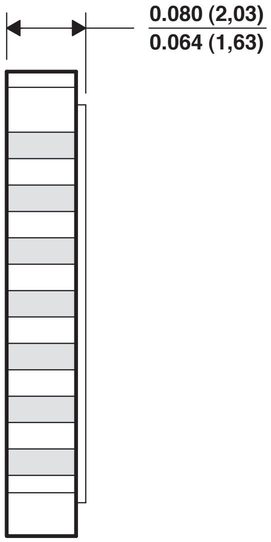
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

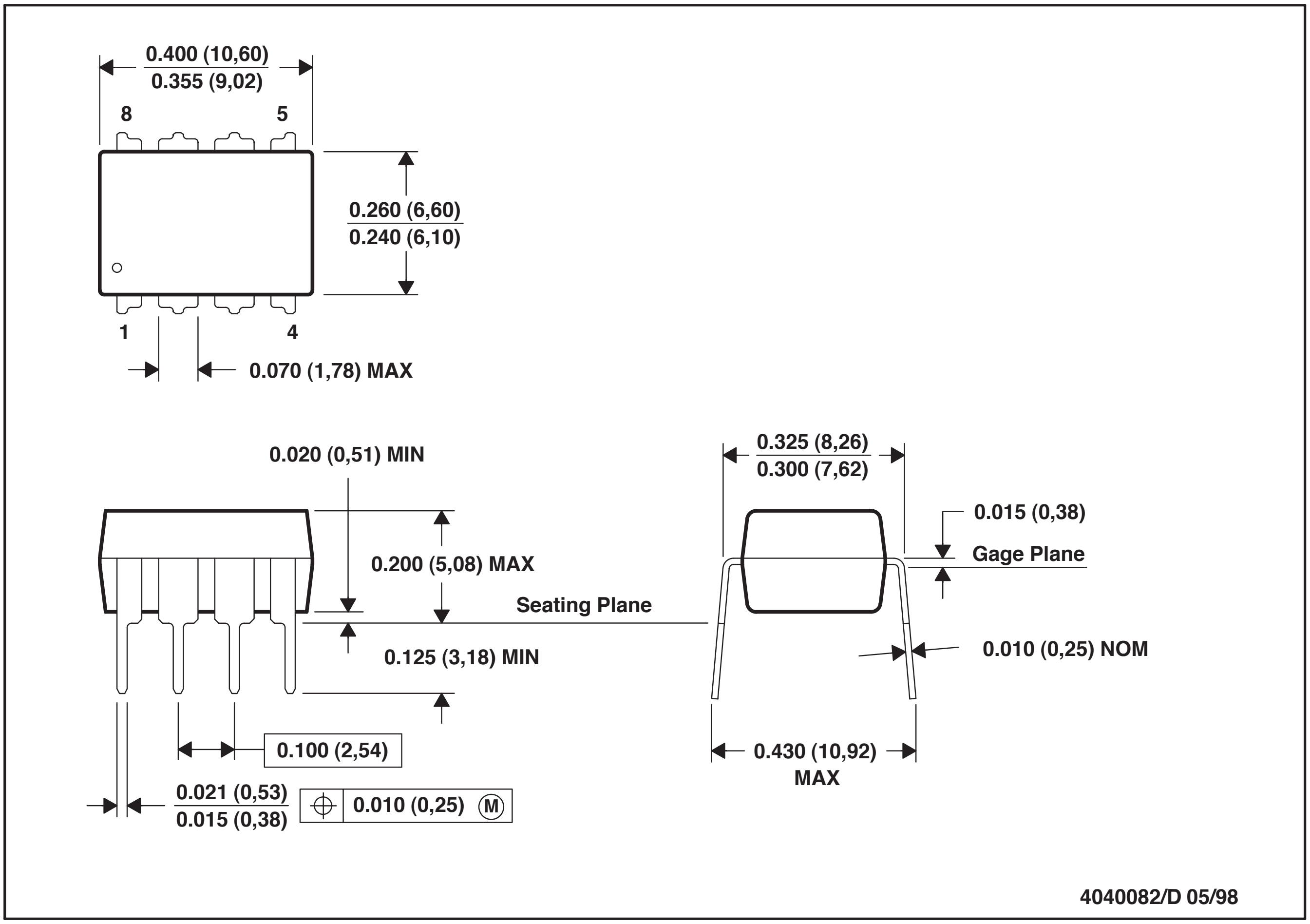




4040140/D 10/96

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**

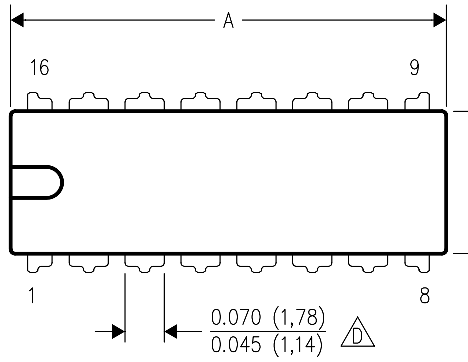


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

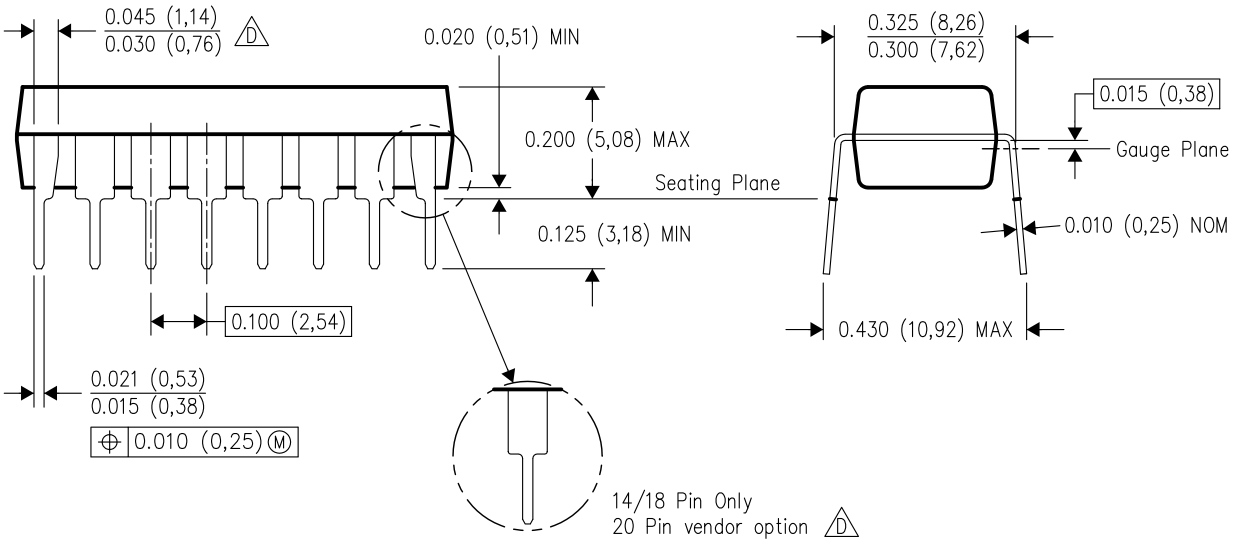
For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



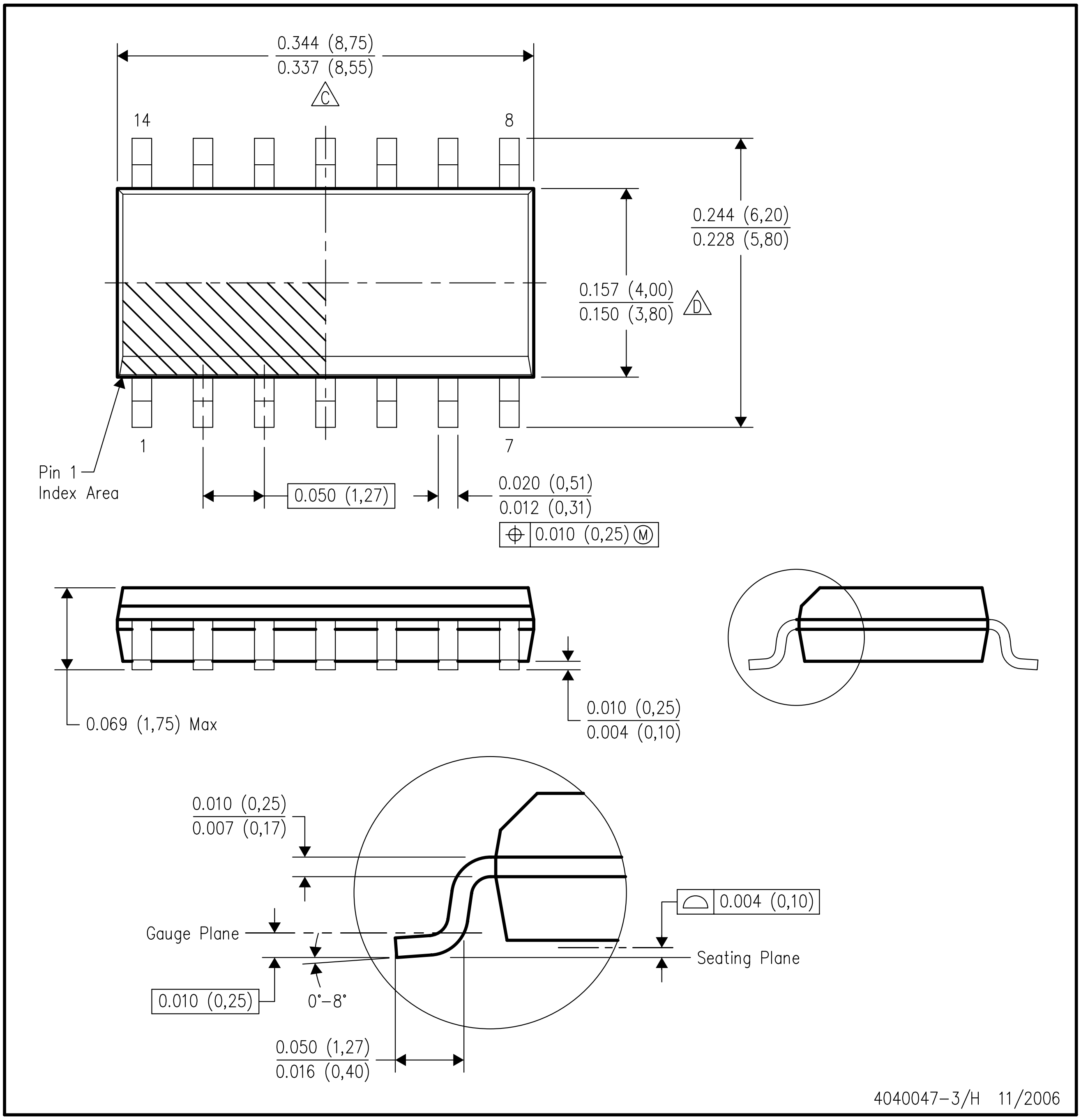
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

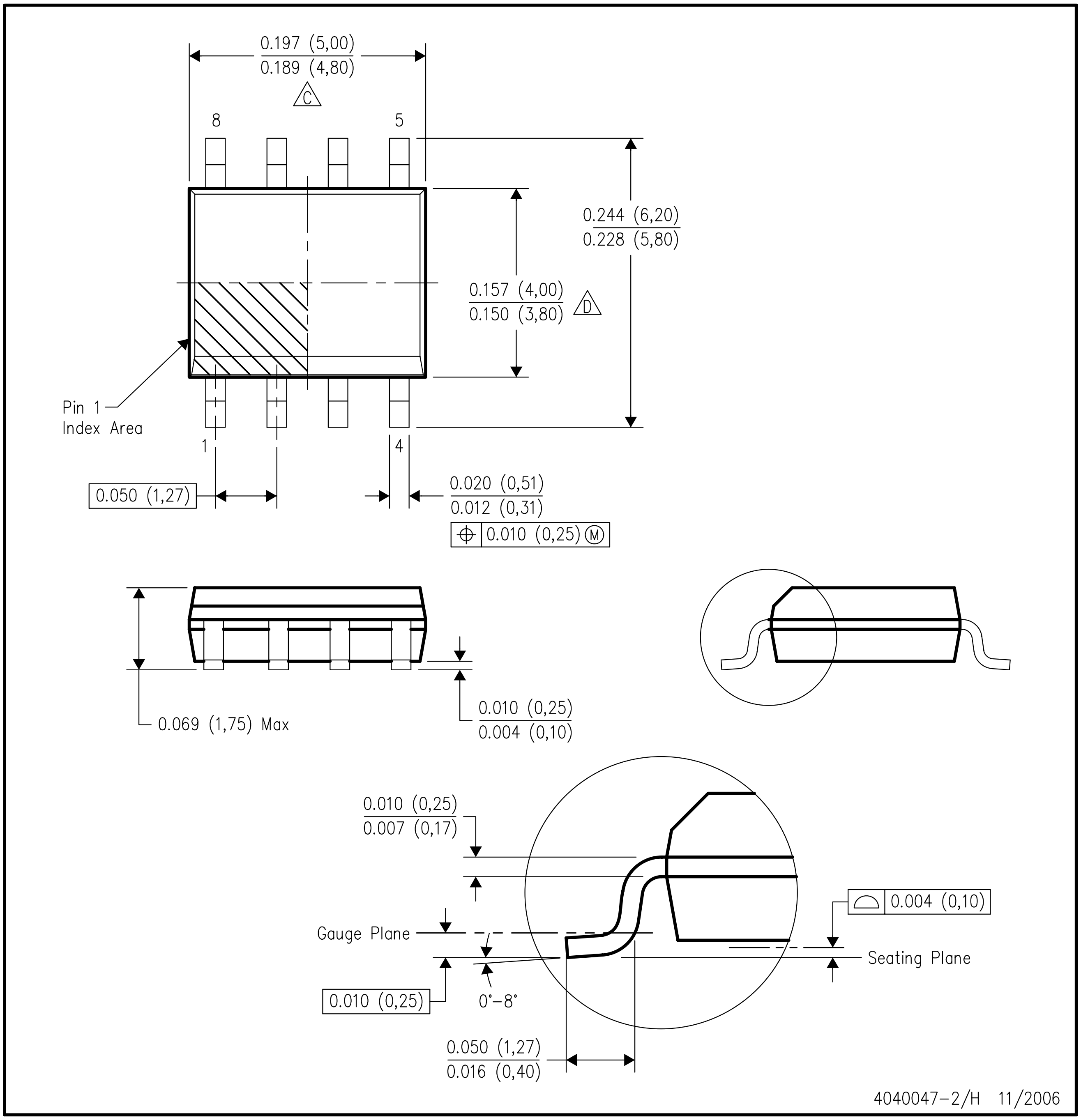
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

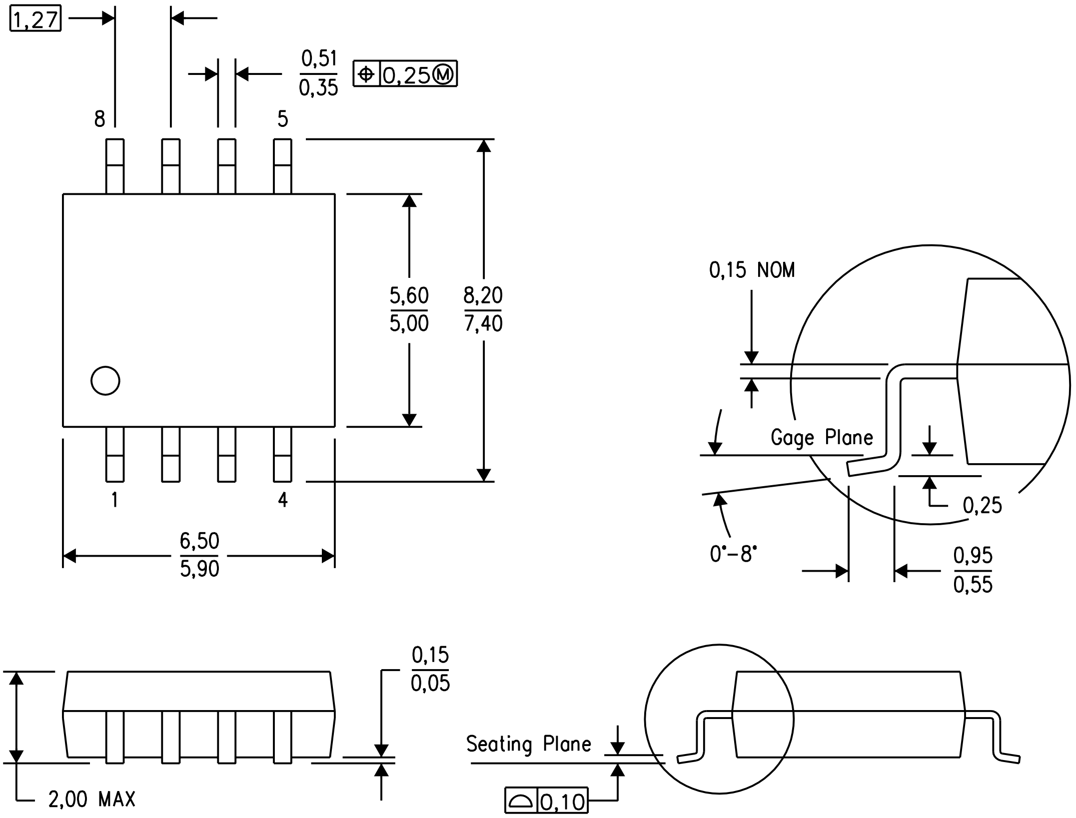


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.



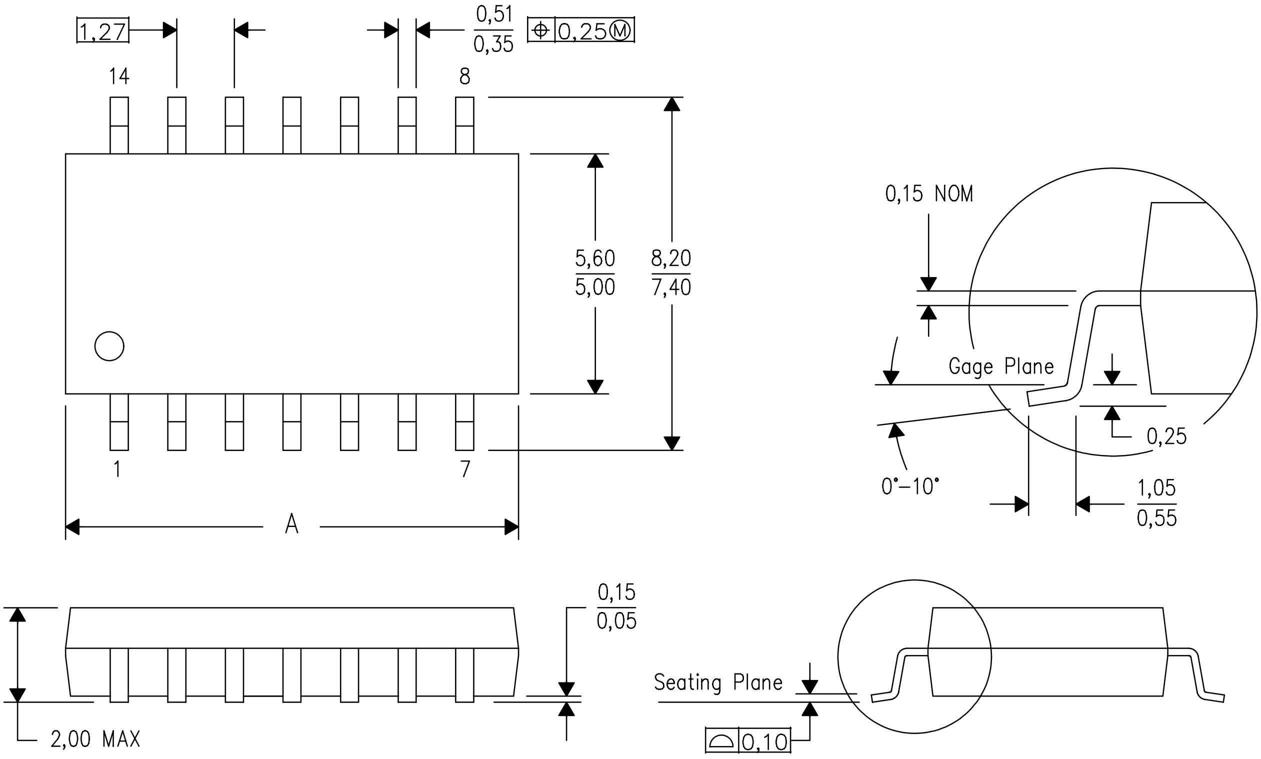
4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



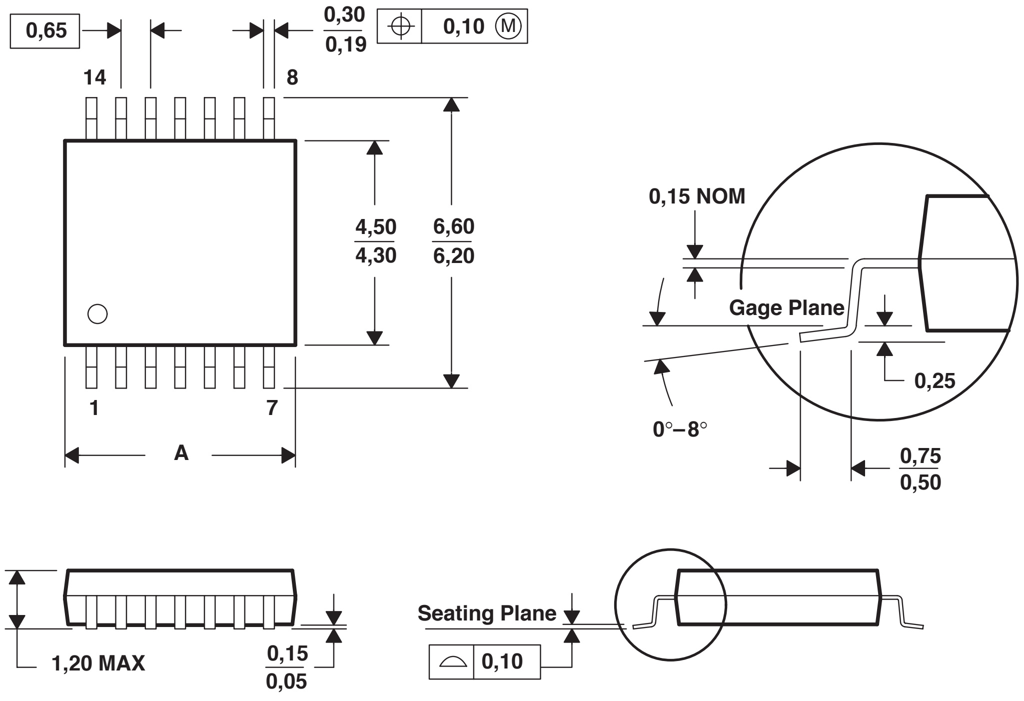
PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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